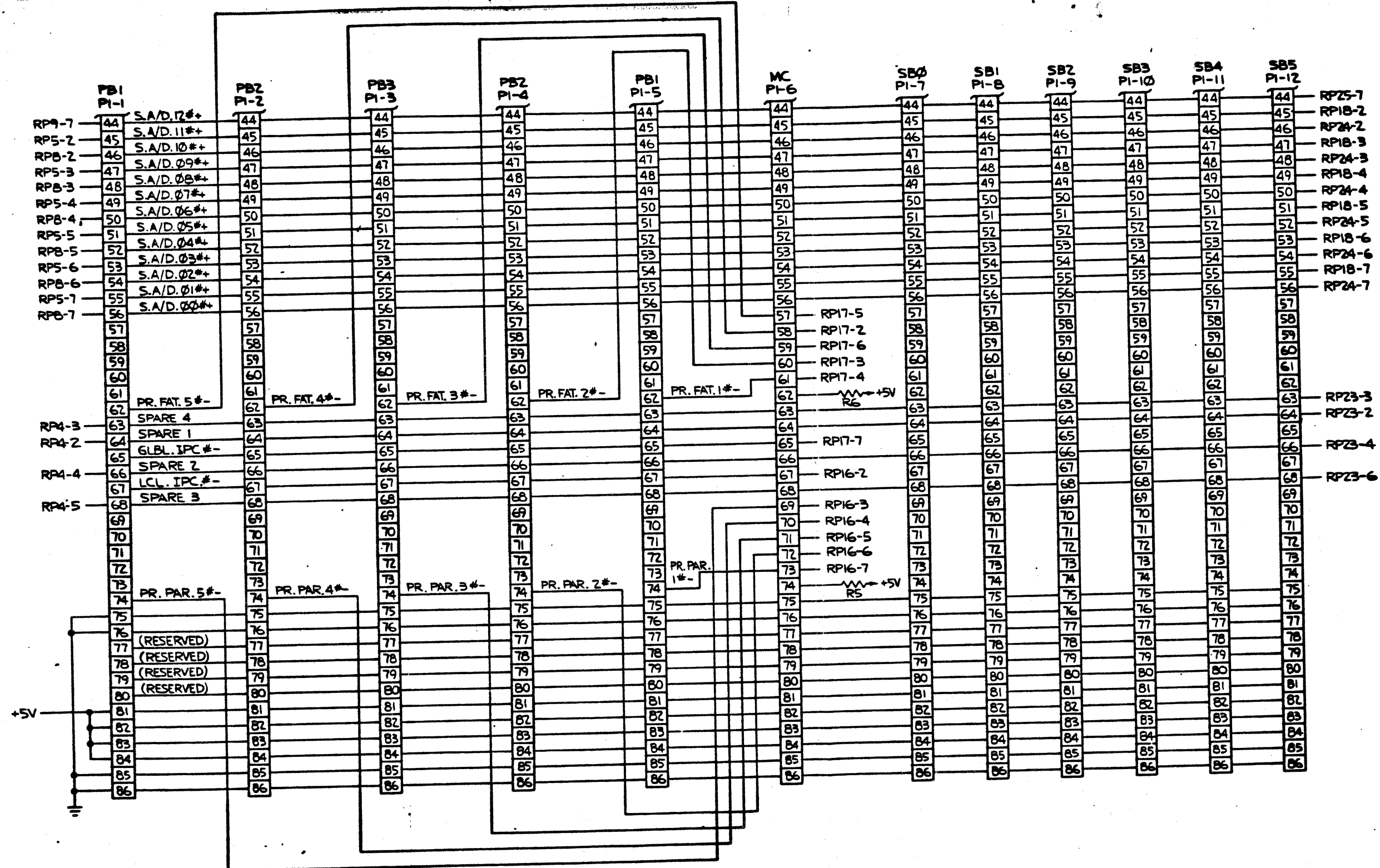


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DATE REV. BY DESCRIPTION

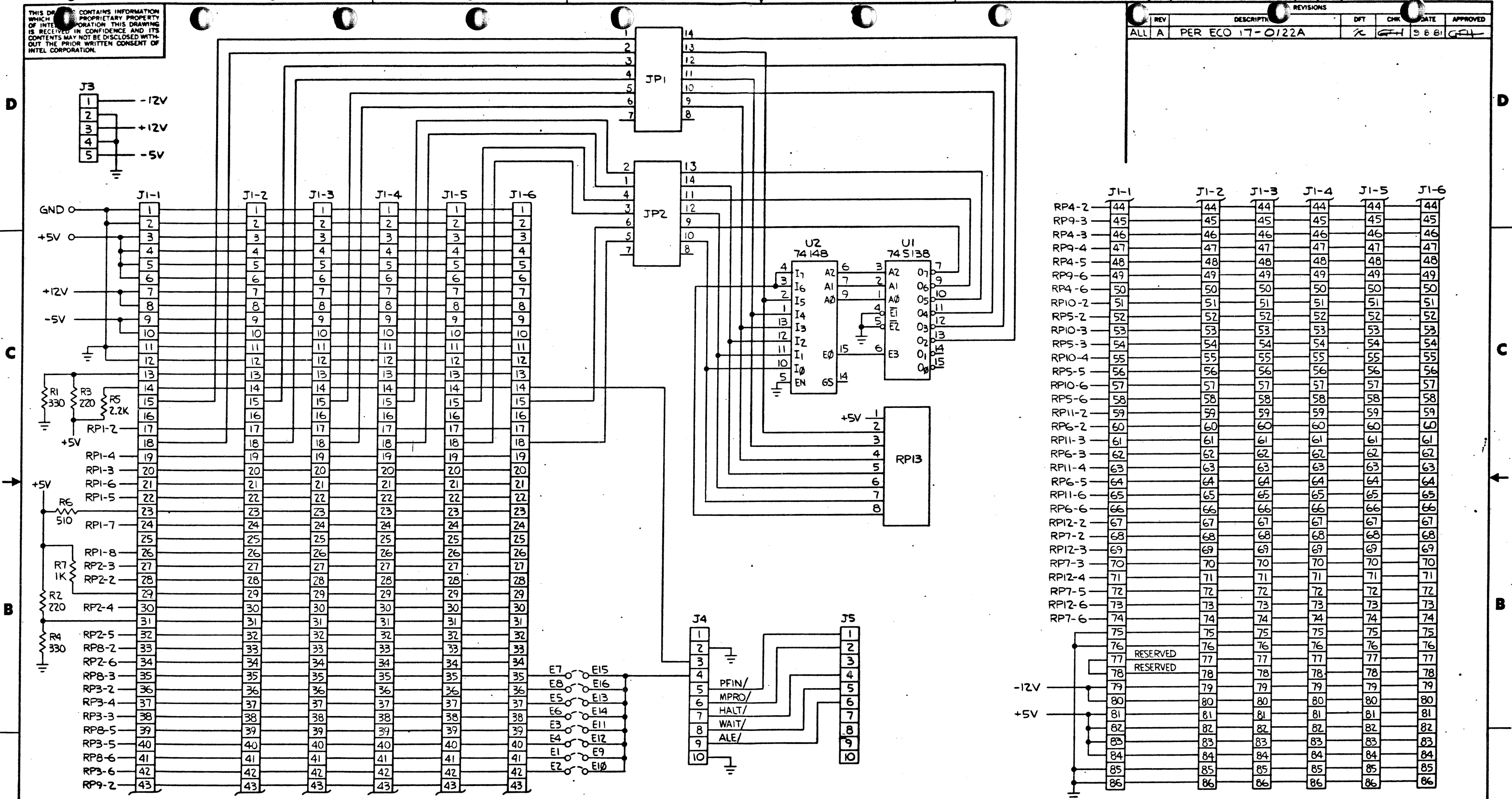


DRAWN J. CHRISTIAN	SIZE D	CODE	DWG NO. 172006	REV B
ISSUED	SCALE		SHEET 2	

8 7 6 5 4 3 2 1

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REV		DESCRIPTION	DFT	CHK	DATE	APPROVED
ALL	A	PER ECO 17-0122A			9 6 81	



	J1-1	J1-2	J1-3	J1-4	J1-5	J1-6
RP4-2	44	44	44	44	44	44
RP9-3	45	45	45	45	45	45
RP4-3	46	46	46	46	46	46
RP9-4	47	47	47	47	47	47
RP4-5	48	48	48	48	48	48
RP9-6	49	49	49	49	49	49
RP4-6	50	50	50	50	50	50
RP10-2	51	51	51	51	51	51
RP5-2	52	52	52	52	52	52
RP10-3	53	53	53	53	53	53
RP5-3	54	54	54	54	54	54
RP10-4	55	55	55	55	55	55
RP5-5	56	56	56	56	56	56
RP10-6	57	57	57	57	57	57
RP5-6	58	58	58	58	58	58
RP11-2	59	59	59	59	59	59
RP6-2	60	60	60	60	60	60
RP11-3	61	61	61	61	61	61
RP6-3	62	62	62	62	62	62
RP11-4	63	63	63	63	63	63
RP6-5	64	64	64	64	64	64
RP11-6	65	65	65	65	65	65
RP6-6	66	66	66	66	66	66
RP12-2	67	67	67	67	67	67
RP7-2	68	68	68	68	68	68
RP12-3	69	69	69	69	69	69
RP7-3	70	70	70	70	70	70
RP12-4	71	71	71	71	71	71
RP7-5	72	72	72	72	72	72
RP12-6	73	73	73	73	73	73
RP7-6	74	74	74	74	74	74
	75	75	75	75	75	75
	76	76	76	76	76	76
	77	RESERVED	77	77	77	77
	78	RESERVED	78	78	78	78
	79		79	79	79	79
	80		80	80	80	80
	81		81	81	81	81
	82		82	82	82	82
	83		83	83	83	83
	84		84	84	84	84
	85		85	85	85	85
	86		86	86	86	86

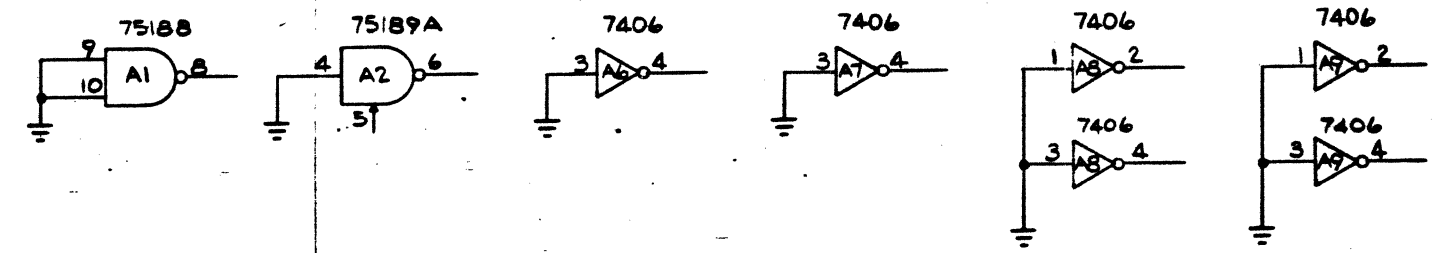
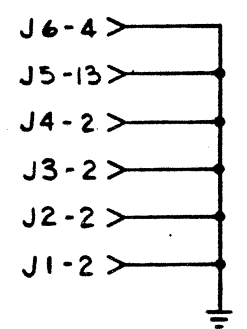
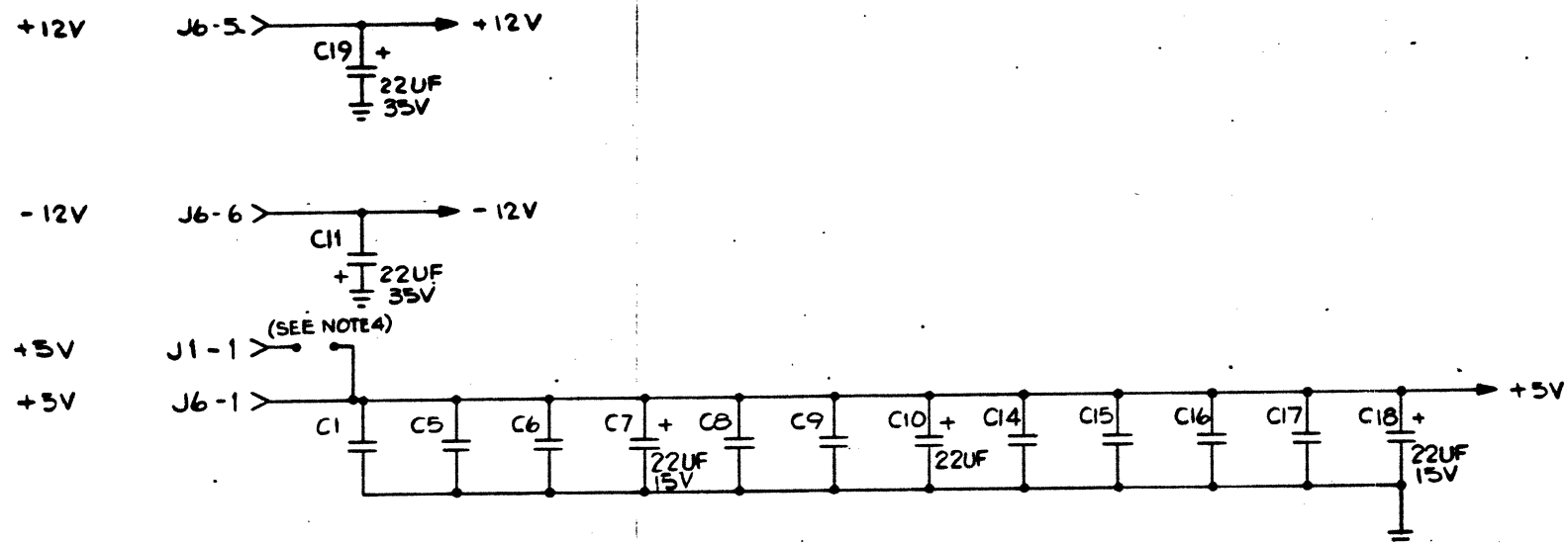
- NOTES UNLESS OTHERWISE SPECIFIED:
1. RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.
 2. RESISTOR PACK (RP) VALUES ARE AS FOLLOWS: RP1, 3, 8 & 13 ARE 1K, RP2, 4-7 & 9-12 ARE 2.2K.
 3. RPX-X DENOTES \rightarrow +5V

ITEM NO.	PART NUMBER	DESCRIPTION
QUANTITY PER DASH NO.		
UNLESS OTHERWISE SPECIFIED:		
DIMENSIONS ARE IN INCHES.		
BREAK ALL SHARP EDGES.		
DO NOT SCALE DRAWING.		
TOLERANCES:		
XX ± .00		
XXX ± .010		
SURFACE FINISH J		
NEXT ASSY	USED ON	

SIGNATURE	DATE	<p>3065 BOWERS AVE. SANTA CLARA, CALIF. 95051</p>
DRN BY J. CHRISTIAN	5/21/81	
CHK BY	7/1/81	
ENGR APVD	7/1/81	
TITLE		<p>SCHMATIC DIAGRAM - PWA, LSBC 432/615; BP6, M-BUS</p>
SIZE	CODE	
D		DWG. NO.
		172226
SCALE		SHEET 1 OF 1

THIS DRAWING CONTAINS INFORMATION WHICH IS PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

REV	DESCRIP	REVISIONS	DFT	DATE	APPROVED
A	PER ECO 17-0147	1 A	BVE	10/21/81	RS



DEVICE TABLE						
REFERENCE DESIGNATION	DEVICE TYPE	GND PIN	+5V PIN	+12V PIN	-12V PIN	UNUSED OUTPUT PINS
A6, A7, A8, A9	7406	7	14			A6-4, A7-4, A8-2,4, A9-2,4
A1	75188	7	14	1		A1-8
A2	75189A	7	14			A2-6
A3, A5	8243	12	24			
A4	8748	20	26,40			
RP1, RP2, RP3, RP4, RP5	R-PACK		1			

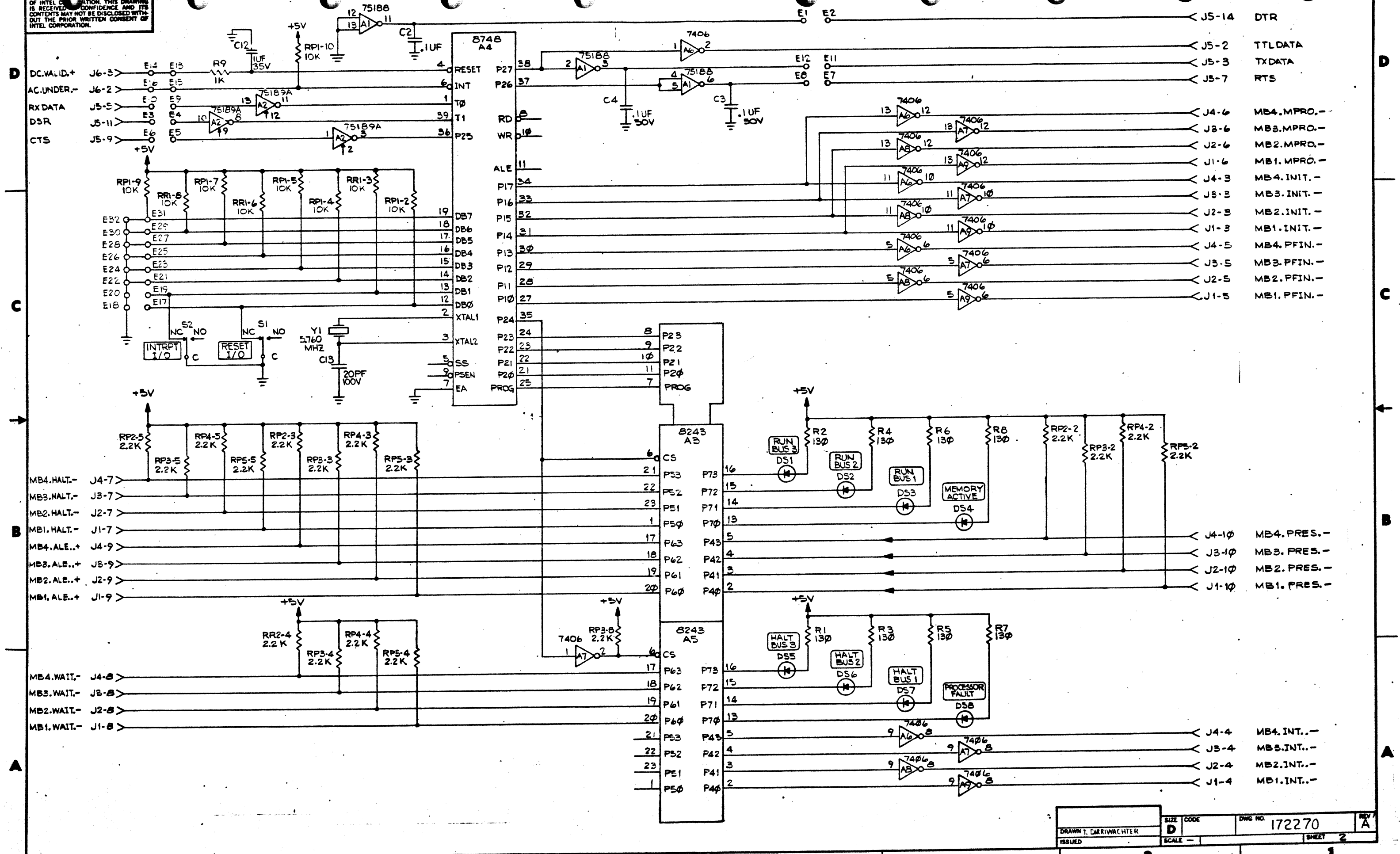
- NOTES UNLESS OTHERWISE SPECIFIED:
- CAPACITORS ARE .01UF, ±20%, 15V.
 - RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W.
 - RESISTOR NETWORKS RP1 THRU RP5 ARE ±5%, 1/4W.
 - OPTIONAL SOURCE FOR +5V.
 - ← DENOTES FLOW DIRECTION

REFERENCE DESIGNATION	QUANTITY	USED ON
Y1		
S2		
RP5		
R9		
J6		
E32		
DS8		
C19		
A9		
LAST USED	NOT USED	

ITEM NO.	PART NUMBER	DESCRIPTION
PARTS LIST		
SIGNATURE		DATE
DRN BY B. VANZYL		10/21/81
CHK BY		10/21/81
ENGR APVD R. Reid		10/21/81
APVD		
APVD		
TITLE		LOGIC DIAGRAM, PWA, SL
SIZE	CODE	DWG. NO. 172270
D		REV A
SCALE NONE		SHEET 1 OF 2

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REV	DESCRIPTION	REVISIONS	DFT	CHK	APPROVED
1					



J5-14	DTR
J5-2	TTLDATA
J5-3	TXDATA
J5-7	RTS
J4-6	MB4.MPRO.-
J3-6	MB3.MPRO.-
J2-6	MB2.MPRO.-
J1-6	MB1.MPRO.-
J4-3	MB4.INIT.-
J3-3	MB3.INIT.-
J2-3	MB2.INIT.-
J1-3	MB1.INIT.-
J4-5	MB4.PFIN.-
J3-5	MB3.PFIN.-
J2-5	MB2.PFIN.-
J1-5	MB1.PFIN.-

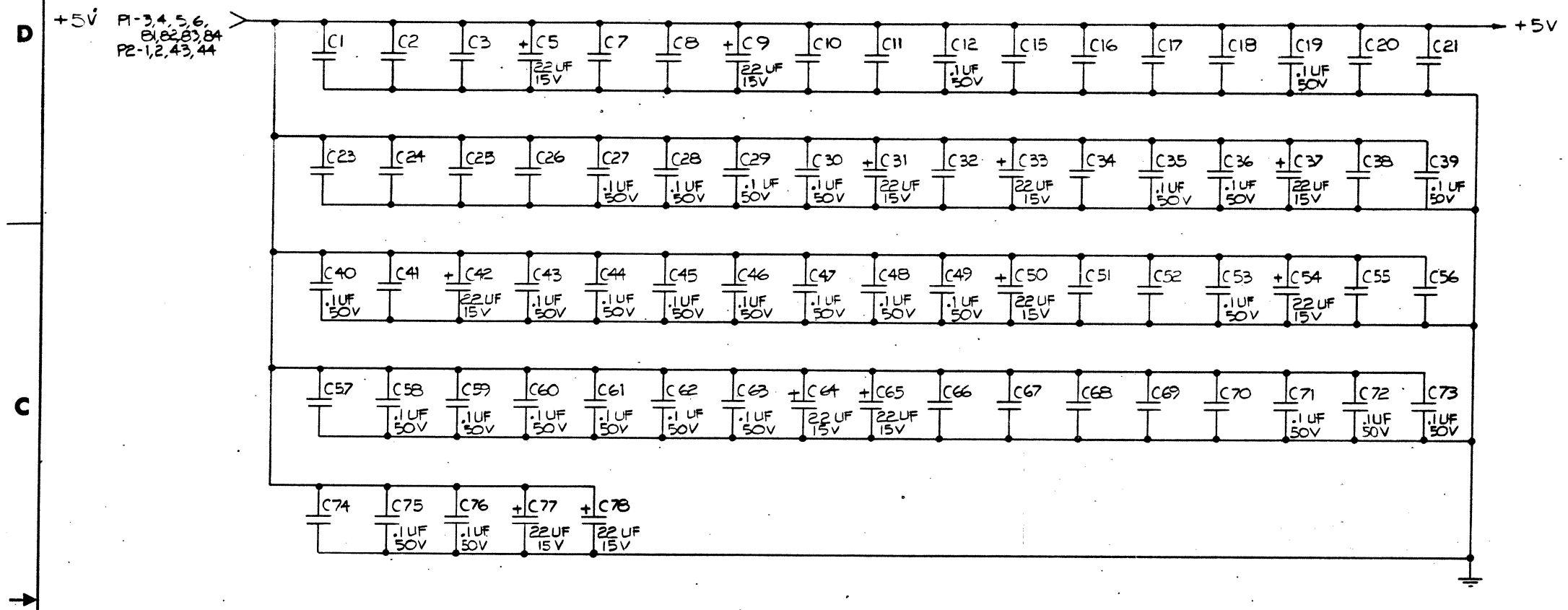
P23	24	8	P23
P22	23	9	P22
P21	22	10	P21
P20	21	11	P20
P19	20	7	P19
P18	19		
P17	18		
P16	17		
P15	16		
P14	15		
P13	14		
P12	13		
P11	12		
P10	11		
P9	10		
P8	9		
P7	8		
P6	7		
P5	6		
P4	5		
P3	4		
P2	3		
P1	2		
P0	1		

DRAWN T. EMRICH	SIZE D	CODE	DWG NO. 172270	REV A
ISSUED	SCALE -		SHEET 2	

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DWG NO. 172320 SH 1 REV A

ZONE	REV	DESCRIPTION	DFT	CHK	DATE	APPROVED
A		PER ECO 17-0212			1/6/82	IS



GND P3-1,3,5,7,9,11, 13,15,17,19,21, 23,25,26,30, 34,38,42,46,50

REFERENCE DESIGNATION	DEVICE TYPE	GND PIN	+5V PIN	UNUSED OUTPUT PINS
E8,H8,K4	74S02	7	14	K4-6
F11,K8	74S02	7	14	
F12,H11,J2	74S04	7	14	F12-6
H6	74LS04	7	14	
H7	74LS27	7	14	
C1,F10,K9	74S51	7	14	C1-8
F9	74S74	7	14	
H9,J1	74S109	8	16	
J10,K7	74LS109	8	16	
J8	74S112	8	16	
G10,H10	74LS138	8	16	
J7,K6	74S151	8	16	
G11	74LS151	8	16	
D1,J3	74S153	8	16	
H5,K10	74S174	8	16	
K5	74LS175	8	16	
J11	74S240	10	20	
A4,A11,B1,B4,B11,C2,C11,D11,E10,E11,G12	74S241	10	20	
J12	74LS244	10	20	
G7,J5,K12	74LS273	10	20	
B2,C3	74S280	7	14	
A2,B3	74S373	10	20	
D2,E6,E7,G8,K3	74S374	10	20	
A10,A12,B10,B12,C4,C10,C12,D4,D10,D12,E9,E12,H12,J9	74LS374	10	20	
D3	74LS377	10	20	
A5,A6,A7,A8,B5,B6,B7,B8,D5,D6,D7,D8	74LS670	8	16	
A9,B9,C5,C6,C7,C8,C9,D9,E5	25S10	8	16	
J6	27S21C	8	16	
F5,F6,F7,F8,G5,G6,H3,H4,J,K11	27S13C	8	16	
G9	PE20102	8	16	
K2	MK1100A	8	16	
F4	43201	8,24,60,64	15,32,50,62	
G4	43202	6,35,39,57,24	2,15,38,50	
RP1,RP2,RP3,RP4			1	

NOTES UNLESS OTHERWISE SPECIFIED:
 1. CAPACITORS ARE .01 UF, 50V.
 2. RESISTANCE IS IN OHMS.

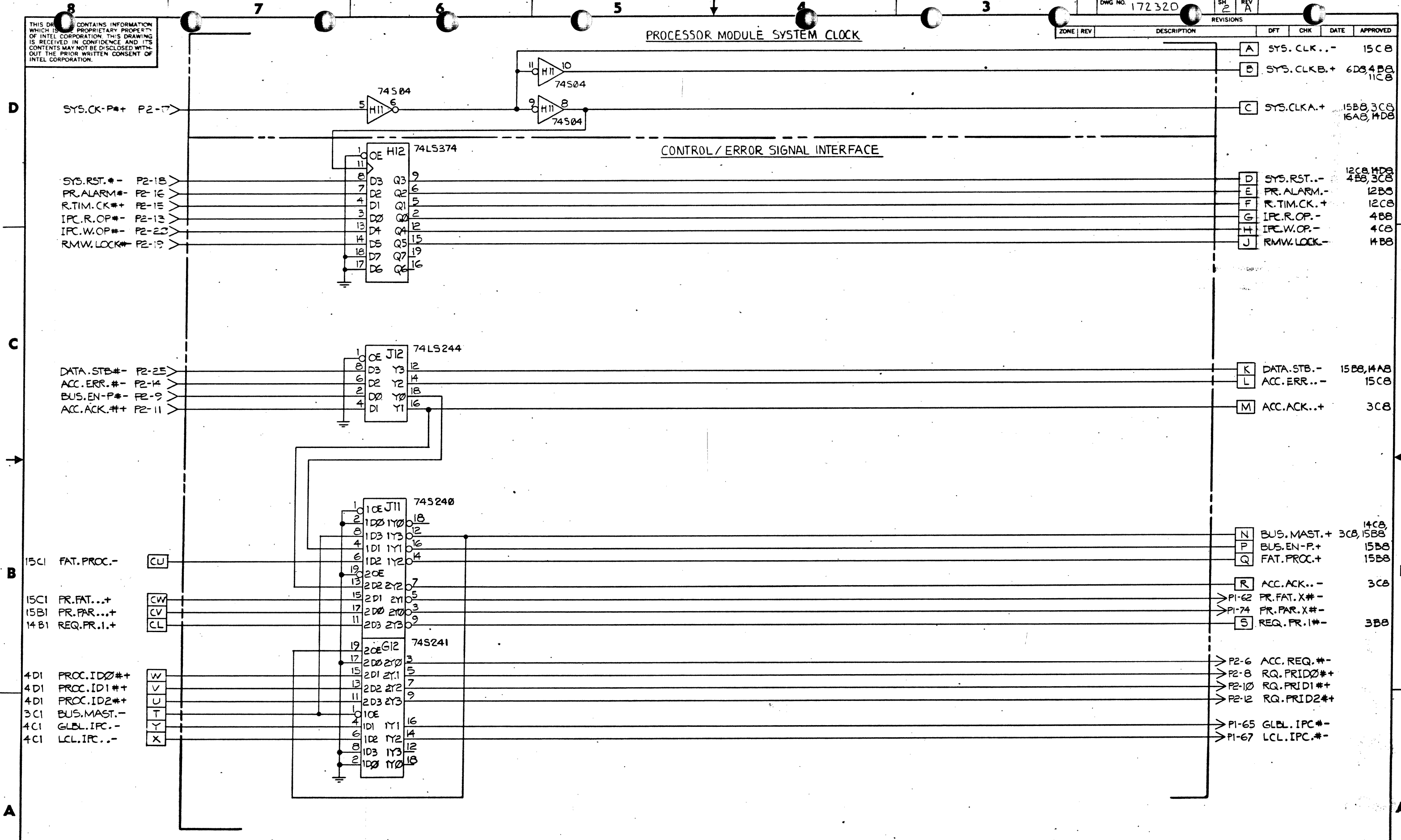
QUANTITY PER DASH NO.	
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. BREAK ALL SHARP EDGES. DO NOT SCALE DRAWING. TOLERANCES: ANGLES ± 2° XX ± .03 XXX ± .010 SURFACE FINISH ✓	
NEXT ASSY	USED ON

SIGNATURE	DATE	<p>3065 BOWERS AVE. SANTA CLARA, CALIF. 95051</p>
DRN BY B. VAN ZYL	1/6/82	
CHK BY T. E. Roth	1/6/82	
ENGR APVD T. E. Roth	1/6/82	
TITLE	LOGIC DIAGRAM, PWA, ISBC 432/601, GDP	
SIZE	CODE	DWG NO.
D	D100	172320
SCALE	SHEET 1 OF 17	

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PROCESSOR MODULE SYSTEM CLOCK

DWG NO.	172320	SH	2	REV	A	
REVISIONS						
ZONE	REV	DESCRIPTION	DFT	CHK	DATE	APPROVED



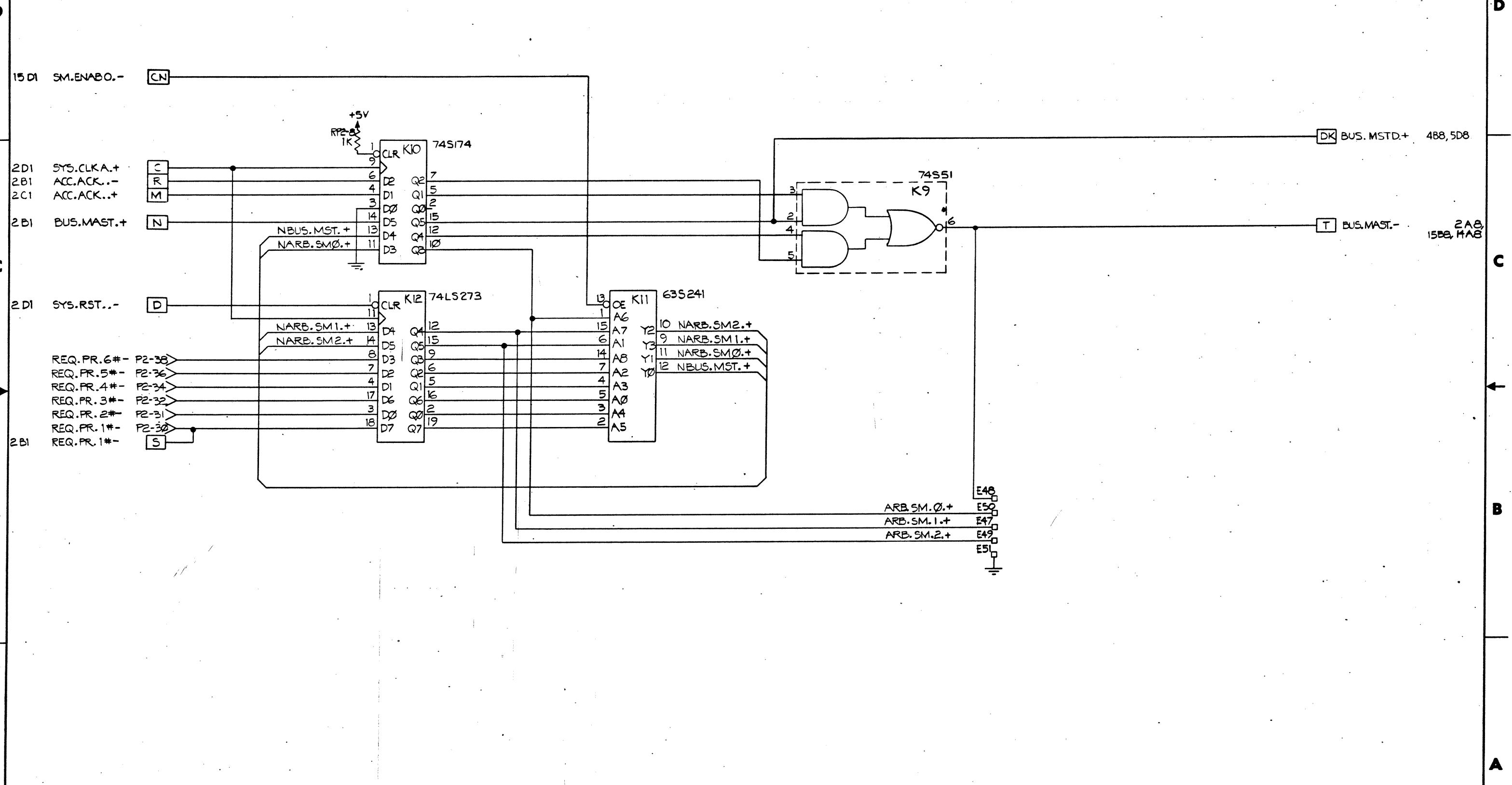
A	SYS.CLK..-	15CB
B	SYS.CLKB.+	6DB, 4BB, 11CB
C	SYS.CLKA.+	15BB, 3CB, 16AB, 14DB
D	SYS.RST..-	12CB, 14DB, 4BB, 3CB
E	PR.ALARM..-	12BB
F	R.TIM.CK.+	12CB
G	IPC.R.OP.-	4BB
H	IPC.W.OP.-	4CB
J	RMW.LOCK.-	4BB
K	DATA.STB.-	15BB, 14AB
L	ACC.ERR..-	15CB
M	ACC.ACK.##	3CB
N	BUS.MAST.+	3CB, 14CB, 15BB
P	BUS.EN-P.+	15BB
Q	FAT.PROC.+	15BB
R	ACC.ACK..-	3CB
	PI-62 PR.FAT.X##	
	PI-74 PR.PAR.X##	
S	REQ.PR.I.##	3BB
	P2-6 ACC.REQ.##	
	P2-8 RQ.PRID0##	
	P2-10 RQ.PRID1##	
	P2-12 RQ.PRID2##	
	PI-65 GLOB.IPC.-	
	PI-67 LCL.IPC.-	

DRAWN	B.VAN ZYL	SIZE	D	CODE		DWG NO.	172320	REV	A
ISSUED		SCALE				SHEET	2		

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DWG NO. 172320		SM 3	REV A
ZONE	REV	DESCRIPTION	DFT
			CHK
			DATE
			APPROVED

ARBITRATION STATE MACHINE

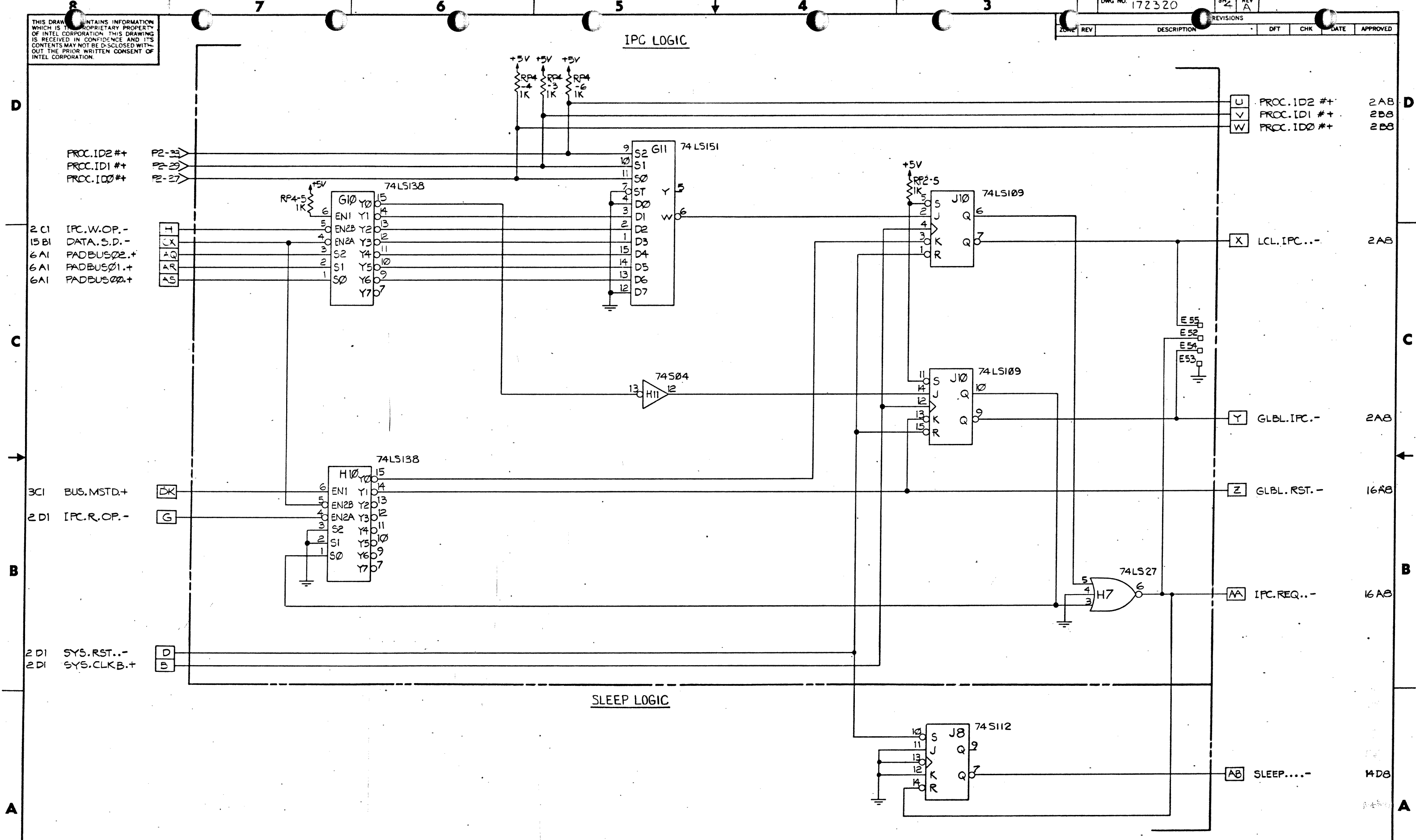


DRAWN B. VAN ZYL	SIZE D	CODE	DWG NO. 172320	REV A
ISSUED	SCALE		SHEET 3	

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DWG NO. 172320		REV A	
ZONE	REV	DESCRIPTION	DATE

IPC LOGIC



U	PROC.ID2 #+	2A8
V	PROC.ID1 #+	2B8
W	PROC.ID0 #+	2B8

X	LCL.IPC...-	2A8
---	-------------	-----

Y	GLBL.IPC.-	2A8
---	------------	-----

Z	GLBL.RST.-	16A8
---	------------	------

AA	IPC.REQ...-	16A8
----	-------------	------

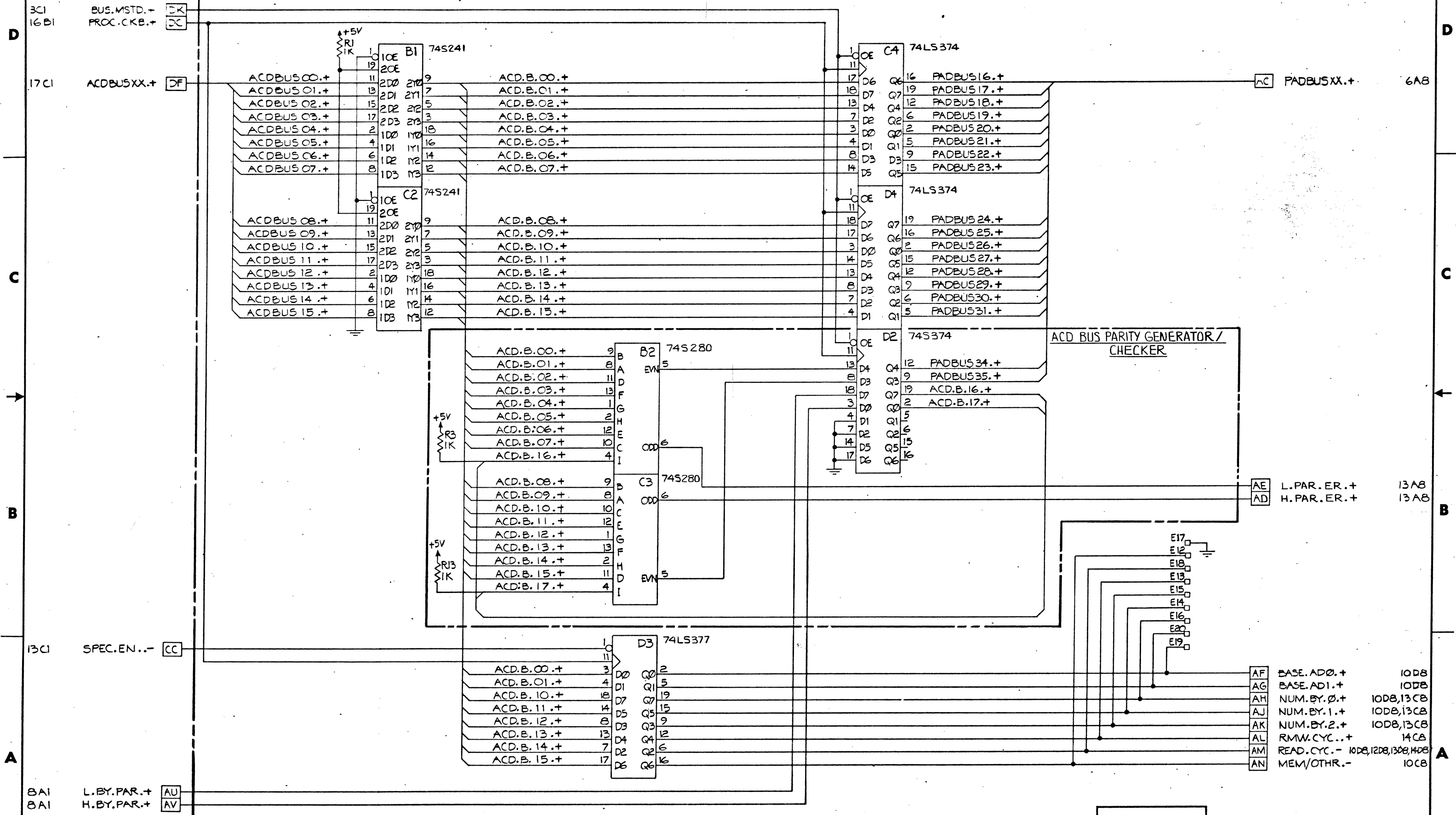
AB	SLEEP....-	14D8
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DRAWN	B.VANZYL	SIZE	D	CODE		DWG NO.	172320	REV	A
ISSUED		SCALE				SHEET	4		

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

ACD BUS OUTPUT INTERFACE

DWG NO. 172320		SH 5	REV A
REVISIONS			
ZONE	REV	DESCRIPTION	DFT
CHK	DATE	APPROVED	



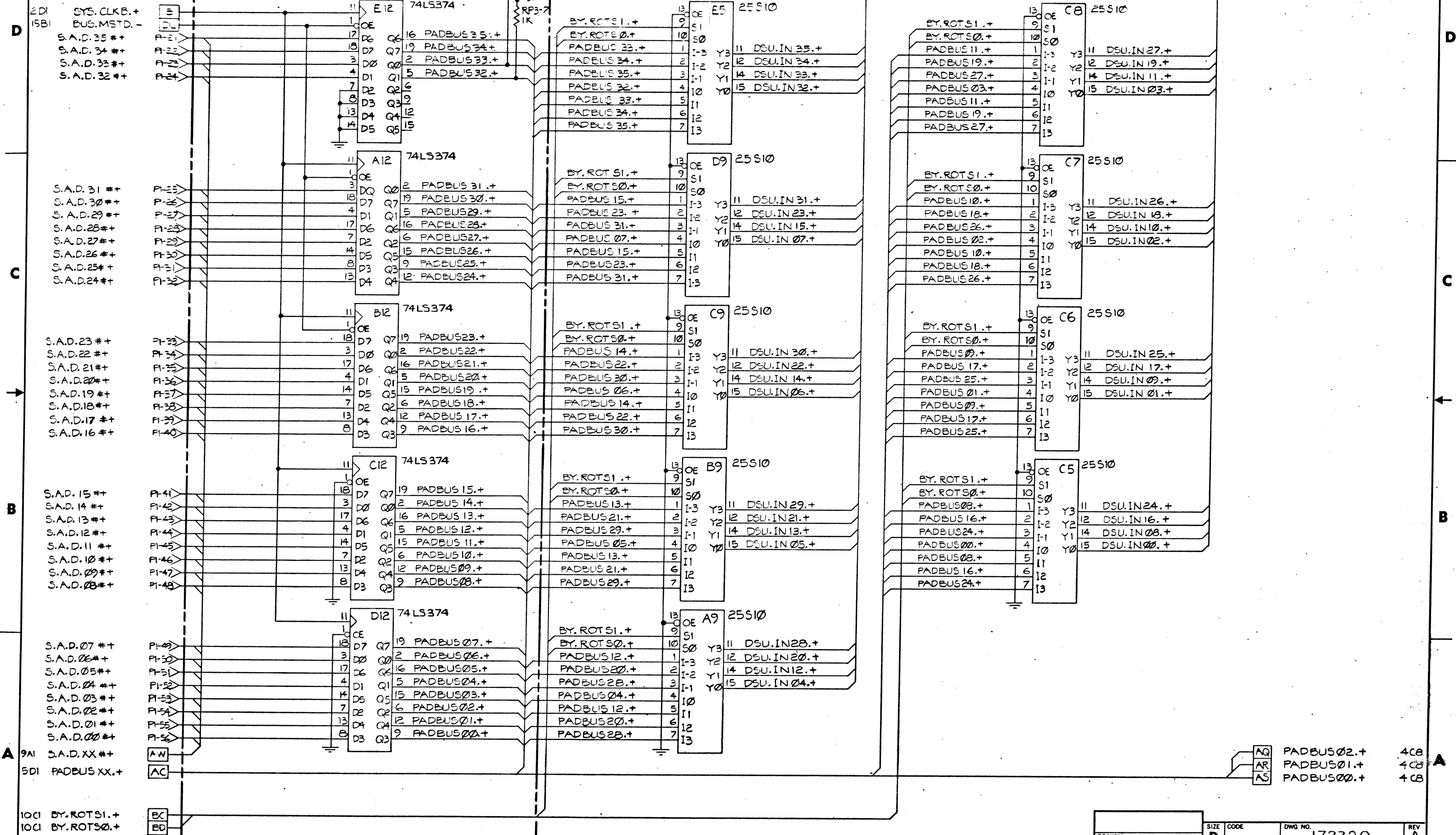
DRAWN B.VAN ZYL	SIZE D	CODE	DWG NO. 172320	REV A
ISSUED	SCALE		SHEET 5	

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

SAD BUS INPUT INTERFACE

DATA ROTATION UNIT

DWG NO.	172320	SH	6	REV	A
REV		DESCRIPTION		DFT	CHK
DATE		APPROVED			



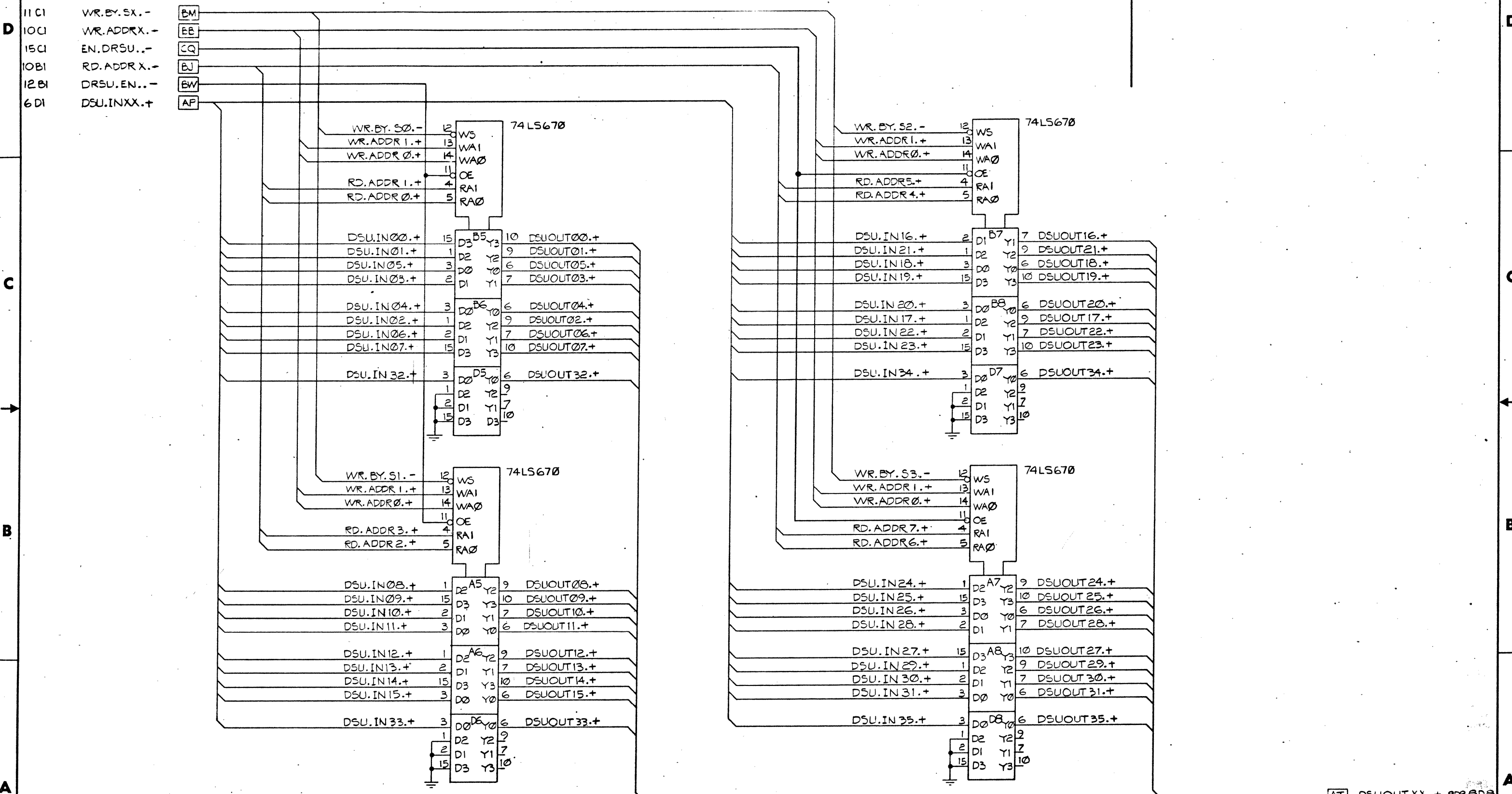
AQ	PABUS02.+	4CB
AR	PABUS01.+	4CB
AS	PABUS00.+	4CB

DRAWN	B.VANZL	SIZE	D	CODE		DWG NO.	172320	REV	A
ISSUED		SCALE				SHEET	6		

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DATA STORAGE UNIT

DWG NO	172320	SM	7	REV	A
REVISIONS					
REV	DESCRIPTION	DFT	CHK	DATE	APPROVED



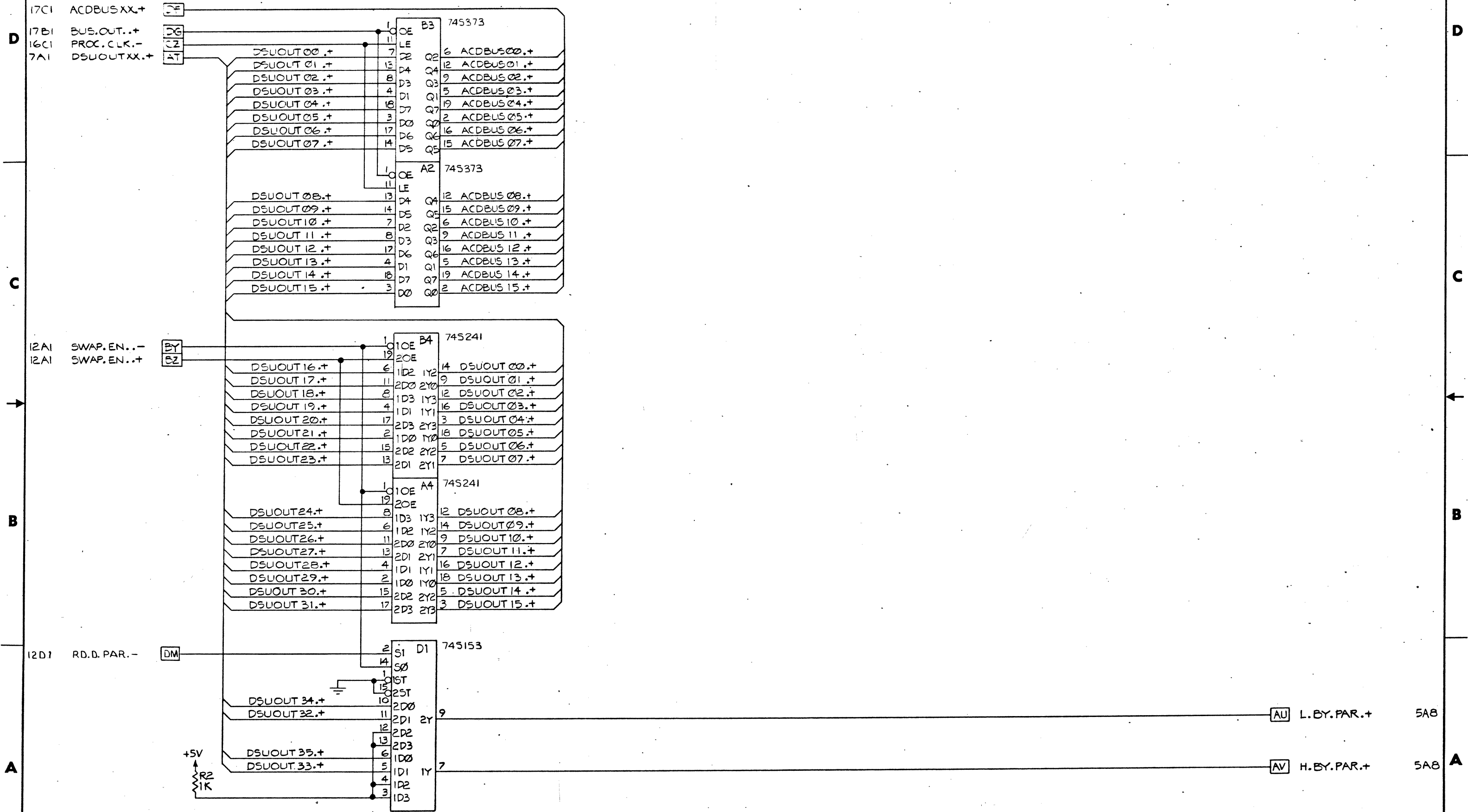
AT DSUOUT XX.+ 908,SDS

DRAWN	B. VAN ZYL	SIZE	CODE	DWG NO.	172320	REV	A
ISSUED		SCALE		SHEET	7		

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

ACD BUS INPUT INTERFACE

DWG NO. 172320		SH E	REV A
REVISIONS			
ZONE	REV	DESCRIPTION	DFT
		CHK	DATE
		APPROVED	



DRAWN B.VAN ZYL	SIZE D	CODE	DWG NO. 172320	REV A
ISSUED	SCALE		SHEET 8	

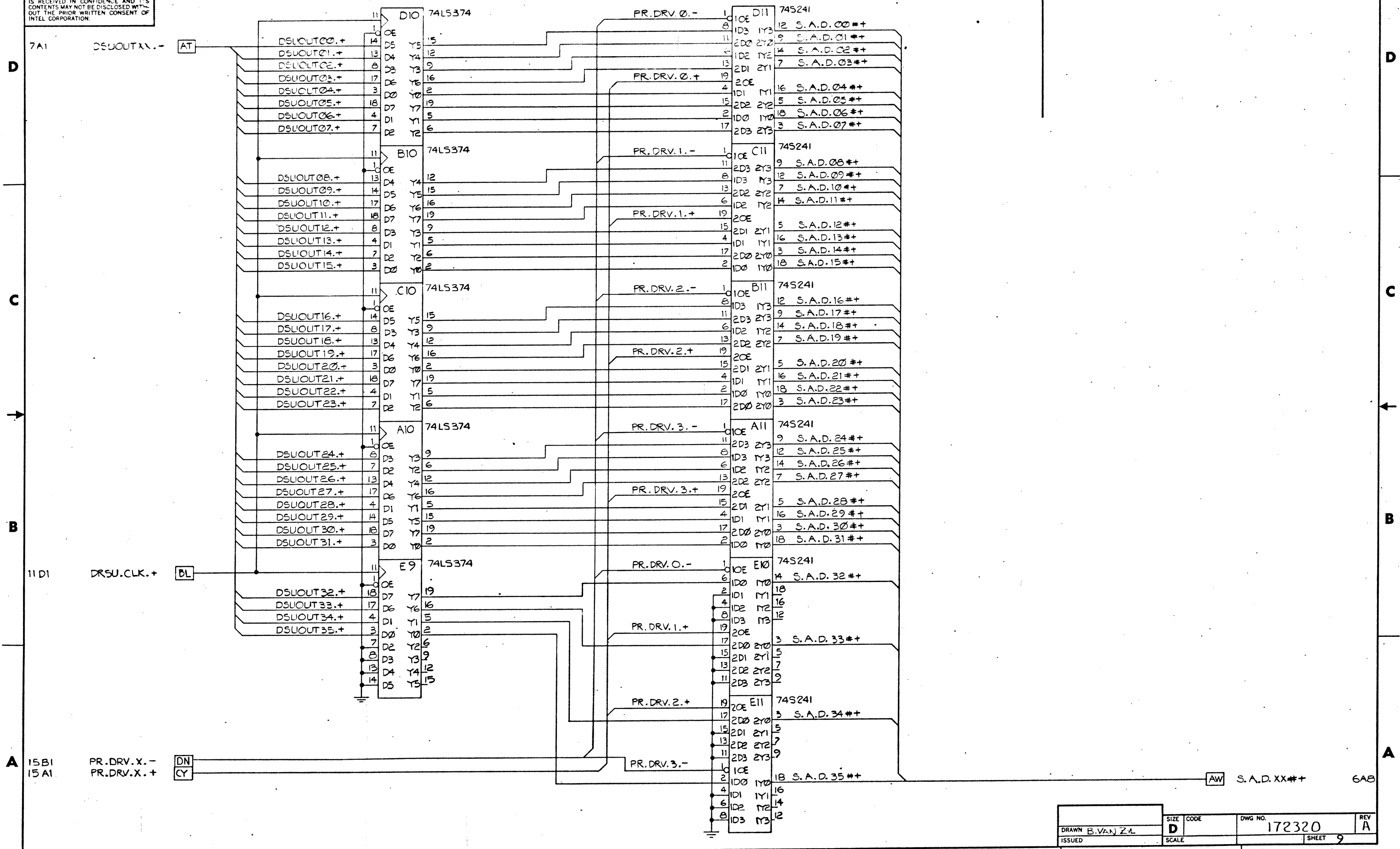
SAD BUS OUTPUT INTERFACE

THIS DRAWING CONTAINS INFORMATION WHICH IS PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

DWG NO. 172320

SH 9 REV A

ZONE	REV	DESCRIPTION	DFT	CHK	DATE	APPROVED

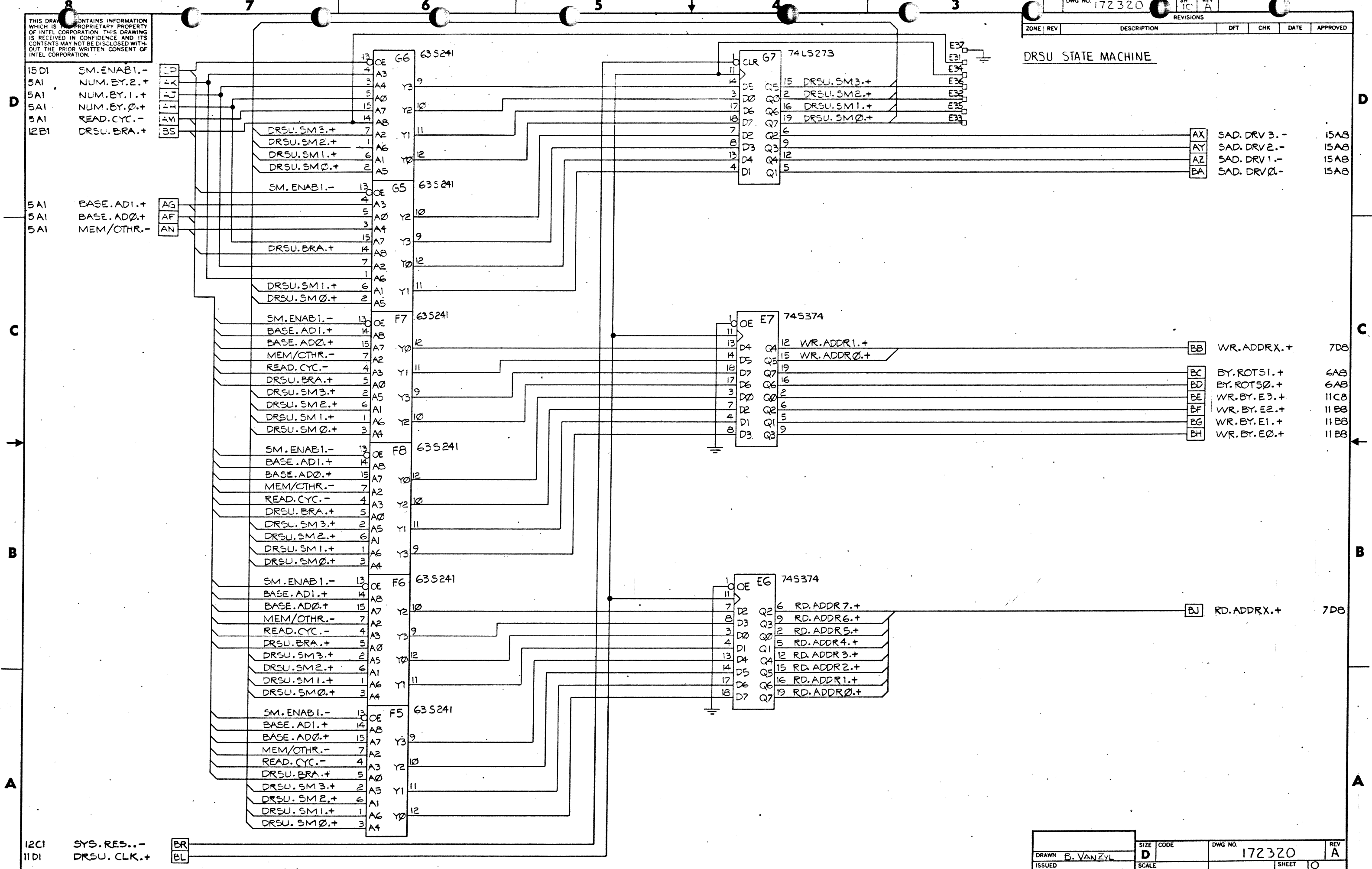


DRAWN B.VAN ZAL	SIZE D	CODE	DWG NO. 172320	REV A
ISSUED	SCALE		SHEET 9	

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

ZONE	REV	DESCRIPTION	DFT	CHK	DATE	APPROVED

DRSU STATE MACHINE



- 15 DI SM.ENABLE-
- 5 AI NUM.BY.2.+
- 5 AI NUM.BY.1.+
- 5 AI NUM.BY.0.+
- 5 AI READ.CYC.-
- 12 BI DRSU.BRA.+
- 5 AI BASE.ADD1.+
- 5 AI BASE.ADD0.+
- 5 AI MEM/OTHR.-
- 12 C1 SYS.RES.-
- 11 DI DRSU.CLK.+

- AX SAD.DRV3.- 15AB
- AY SAD.DRV2.- 15AB
- AZ SAD.DRV1.- 15AB
- BA SAD.DRV0.- 15AB

- BB WR.ADDRX.+ 7DB
- BC BY.ROTS1.+ 6AB
- BD BY.ROTS0.+ 6AB
- BE WR.BY.E3.+ 11CB
- BF WR.BY.E2.+ 11BB
- BG WR.BY.E1.+ 11BB
- BH WR.BY.E0.+ 11BB

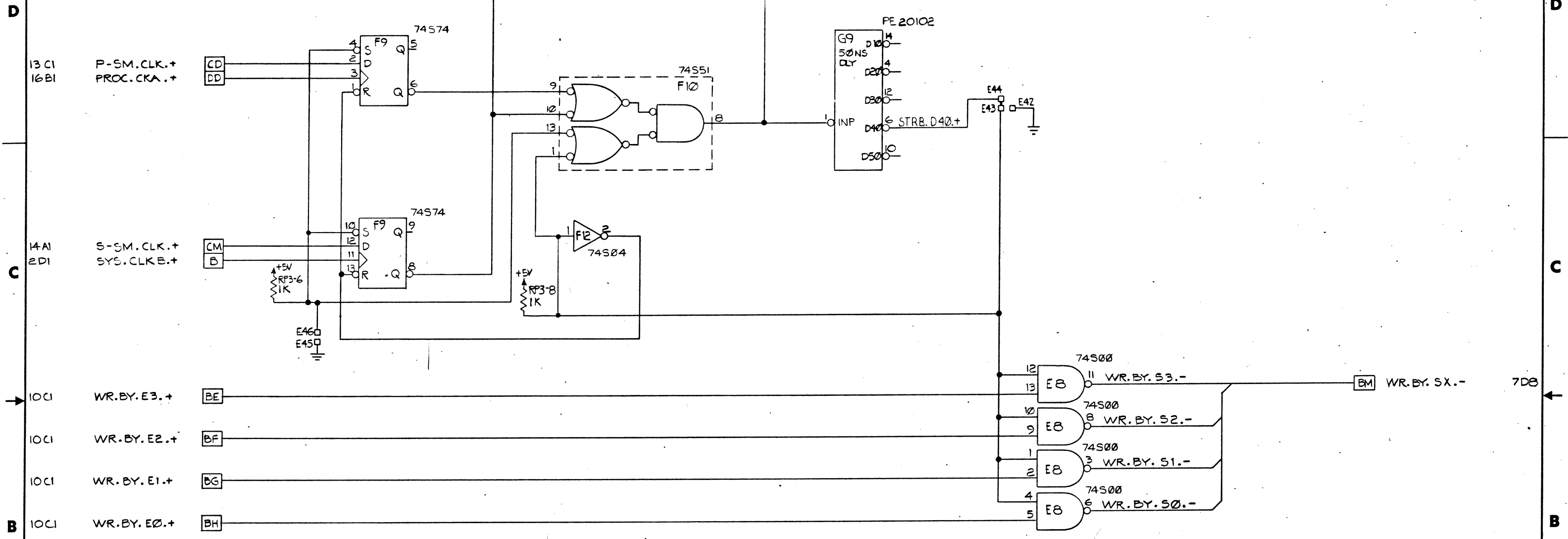
- BJ RD.ADDRX.+ 7DB

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DRSU CLOCK LOGIC

DWG NO. 172320		SH 11	REV A
ZONE	REV	DESCRIPTION	DATE

BK	ERR. CLR.-	15CB
BL	DRSU.CLK.+	10AB,9BB



D

C

B

A

D

C

B

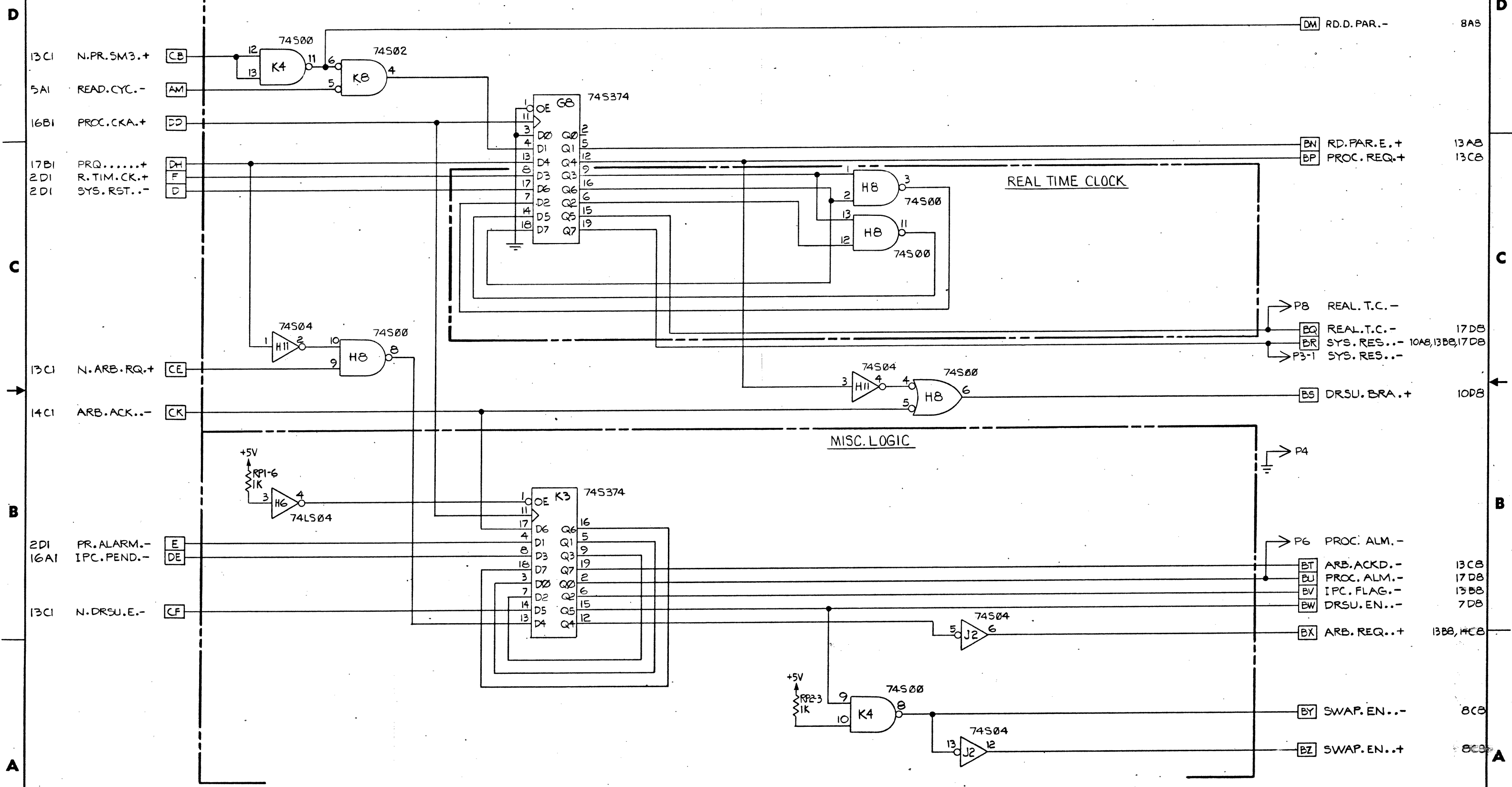
A

DRAWN B.VANZYL	SIZE D	CODE	DWG NO. 172320	REV A
ISSUED	SCALE		SHEET 11	

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PROCESSOR REQUEST LOGIC

DWG NO. 172320		SH 12	REV A
REVISIONS			
ZONE	REV	DESCRIPTION	DFT
CHK	DATE	APPROVED	



- D 13CI N.PR.SM3.+ CB
- D 5AI READ.CYC.- AM
- D 16BI PROC.CKA.+ DD
- D 17BI PRQ.....+ DH
- D 2DI R.TIM.CK.+ F
- D 2DI SYS.RST.- D
- C 13CI N.ARB.RQ.+ CE
- C 14CI ARB.ACK.- CK
- B 2DI PR.ALARM.- E
- B 16AI IPC.PEND.- DE
- A 13CI N.DRSU.E.- CF

- DM RD.D.PAR.- 8AB
- BN RD.PAR.E.+ 13AB
- BP PROC.REQ.+ 13CB
- PB REAL.T.C.-
- BQ REAL.T.C.- 17DB
- BR SYS.RES.- 10AB,13BB,17DB
- P3-1 SYS.RES.-
- BS DRSU.BRA.+ 10DB
- P4
- P6 PROC.ALM.-
- BT ARB.ACKD.- 13CB
- BU PROC.ALM.- 17DB
- BV IPC.FLAG.- 13BB
- BW DRSU.EN.- 7DB
- BX ARB.REQ..+ 13BB,14CB
- BY SWAP.EN.- 8CB
- BZ SWAP.EN.+ 8CB

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PROCESSOR STATE MACHINE

DWG NO 172320		SH 13	REV A
REVISIONS			
ZONE	REV	DESCRIPTION	DFT

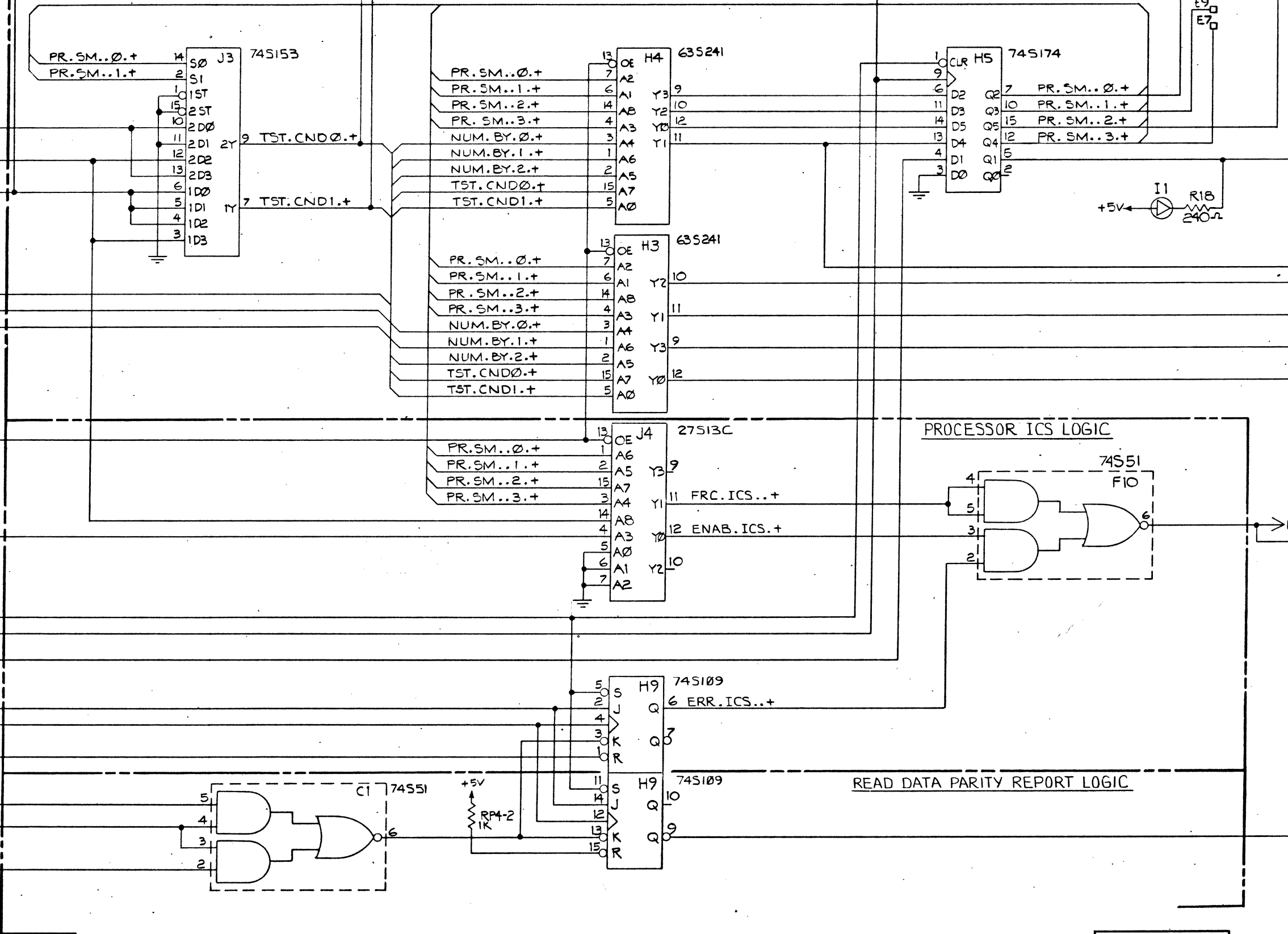
D

C

B

A

- 5A1 READ.CYC.- [AM]
- 12B1 ARB.ACKD.- [BT]
- 12C1 PROC.REQ.+ [BP]
- 5A1 NUM.BY.0.+ [AH]
- 5A1 NUM.BY.1.+ [AJ]
- 5A1 NUM.BY.2.+ [AK]
- 15C1 SM.ENAB3.- [CR]
- 12B1 IPC.FLAG.- [BV]
- 12C1 SYS.RES.- [BR]
- 16B1 PROC.CKB.+ [DC]
- 17A1 FATAL....- [DJ]
- 12A1 ARB.REQ.+ [BX]
- 16C1 PROC.CLK.- [CZ]
- 15C1 MERR.....- [CT]
- 5B1 H.PAR.ER.+ [AD]
- 12C1 RD.PAR.E.+ [BN]
- 5B1 L.PAR.ER.+ [AE]



- [CA] FATAL.PR.- 15B8
- [CB] N.PR.SM3.+ 12D8
- [CC] SPEC.EN...- 16A8,5A8
- [CD] P-SM.CLK.+ 11D8
- [CE] N.ARB.RQ.+ 12CB
- [CF] N.DRSU.E.- 12BB
- [CG] P3-21 ICS.....+ 17D8
- [CH] READ.P.E.+ 15B8

D

C

B

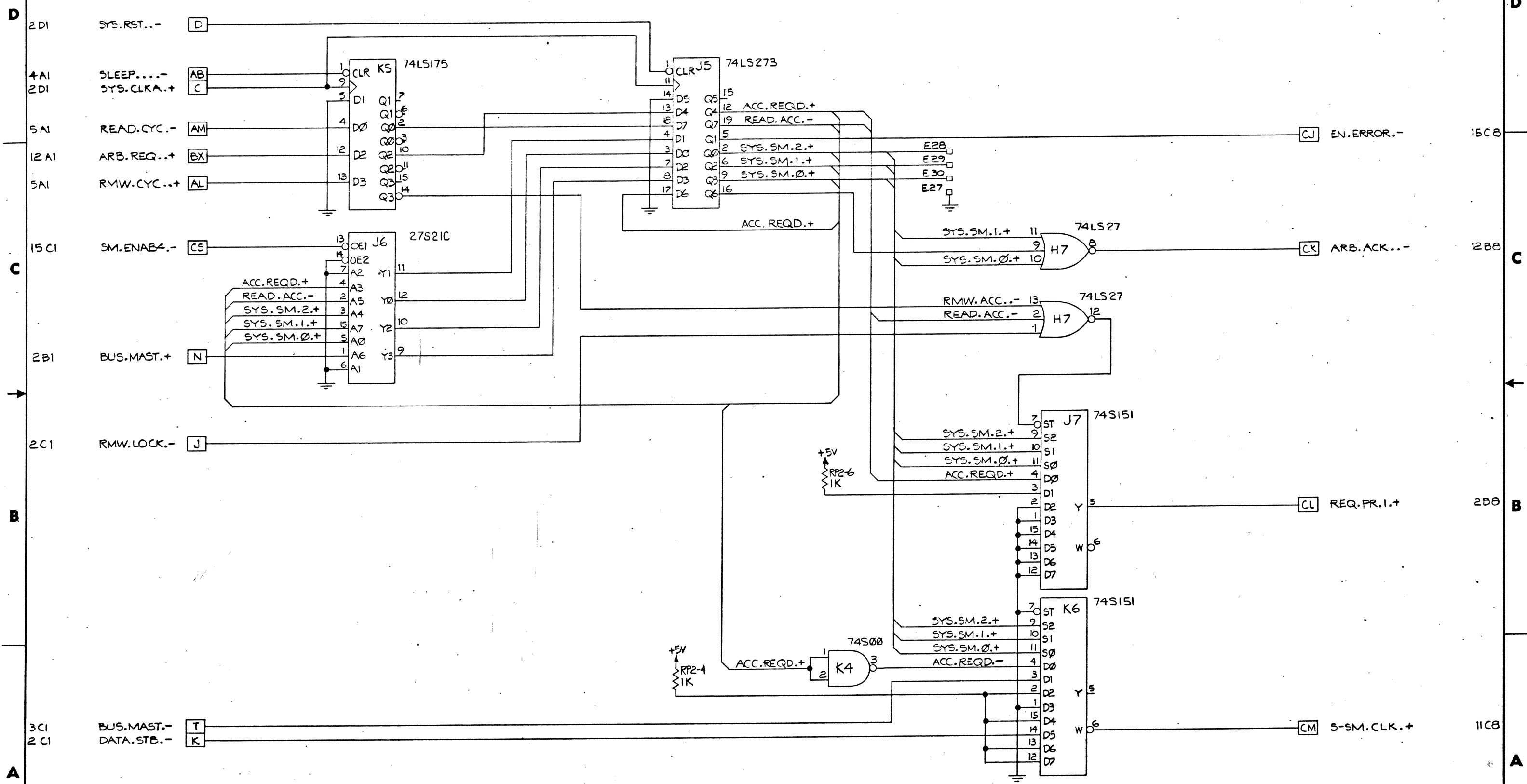
A

DRAWN B.VAN ZYL	SIZE D	CODE	DWG NO. 172320	REV A
ISSUED	SCALE		SHEET 13	

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

DWG NO. 172320		SM 14	REV A
REVISIONS			
ZONE	REV	DESCRIPTION	DFT
CHK	DATE	APPROVED	

SYS BUS STATE MACHINE



DRAWN B. VAN ZYL	SIZE D	CODE	DWG NO. 172320	REV A
ISSUED	SCALE		SHEET 14	

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TESTER CONTROL POINTS

D

D

C

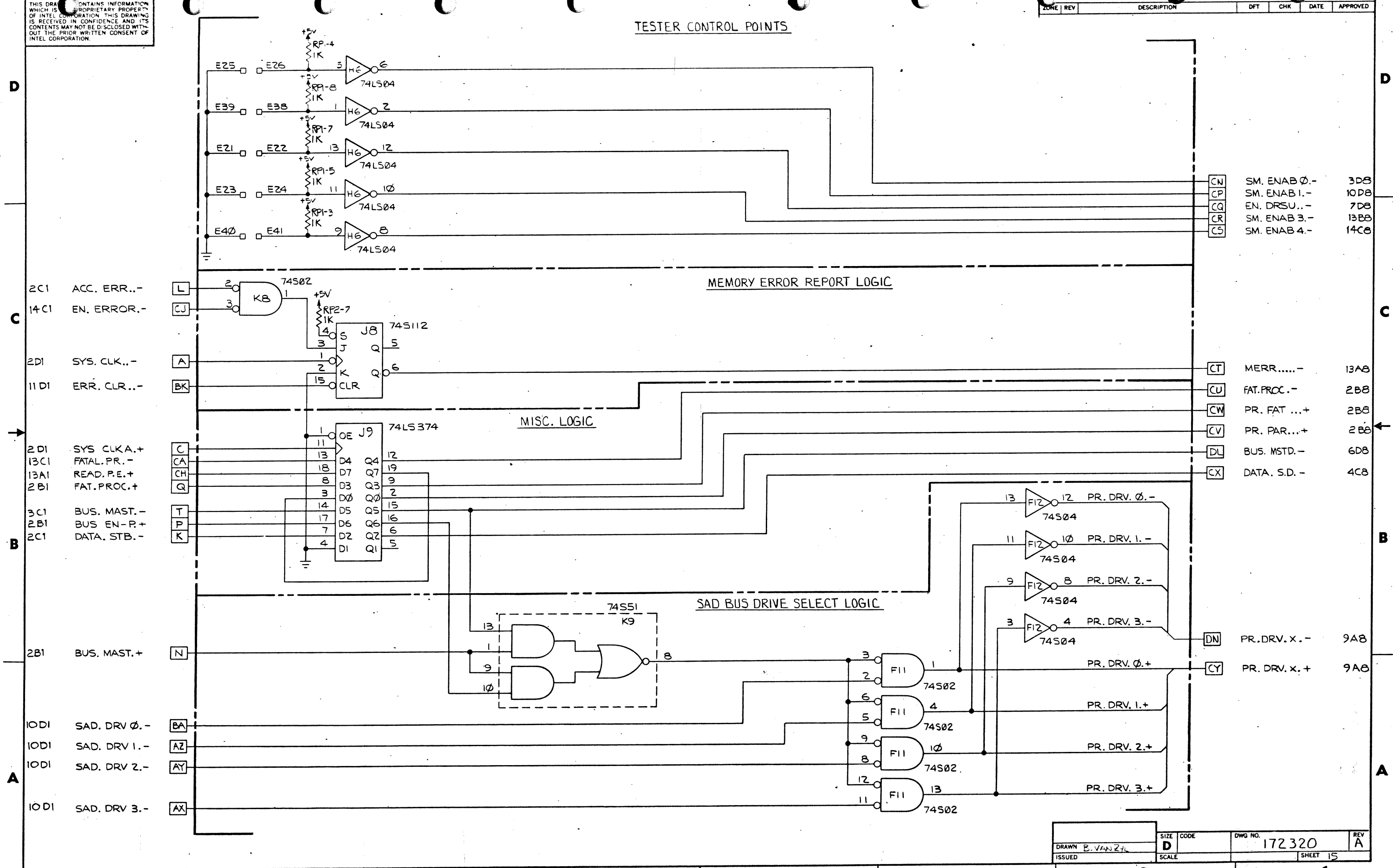
C

B

B

A

A



CN	SM. ENAB 0.-	3DB
CP	SM. ENAB 1.-	10DB
CQ	EN. DRSU...-	7DB
CR	SM. ENAB 3.-	13DB
CS	SM. ENAB 4.-	14CB

CT	MERR.....-	13AB
CU	FAT.PROC.-	2BB
CW	PR. FAT...+	2BB
CV	PR. PAR...+	2BB
DL	BUS. MSTD.-	6DB
CX	DATA. S.D.-	4CB

DN	PR.DRV. X.-	9AB
CY	PR.DRV. X.+	9AB

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43201/02 AND TTL CLOCKS

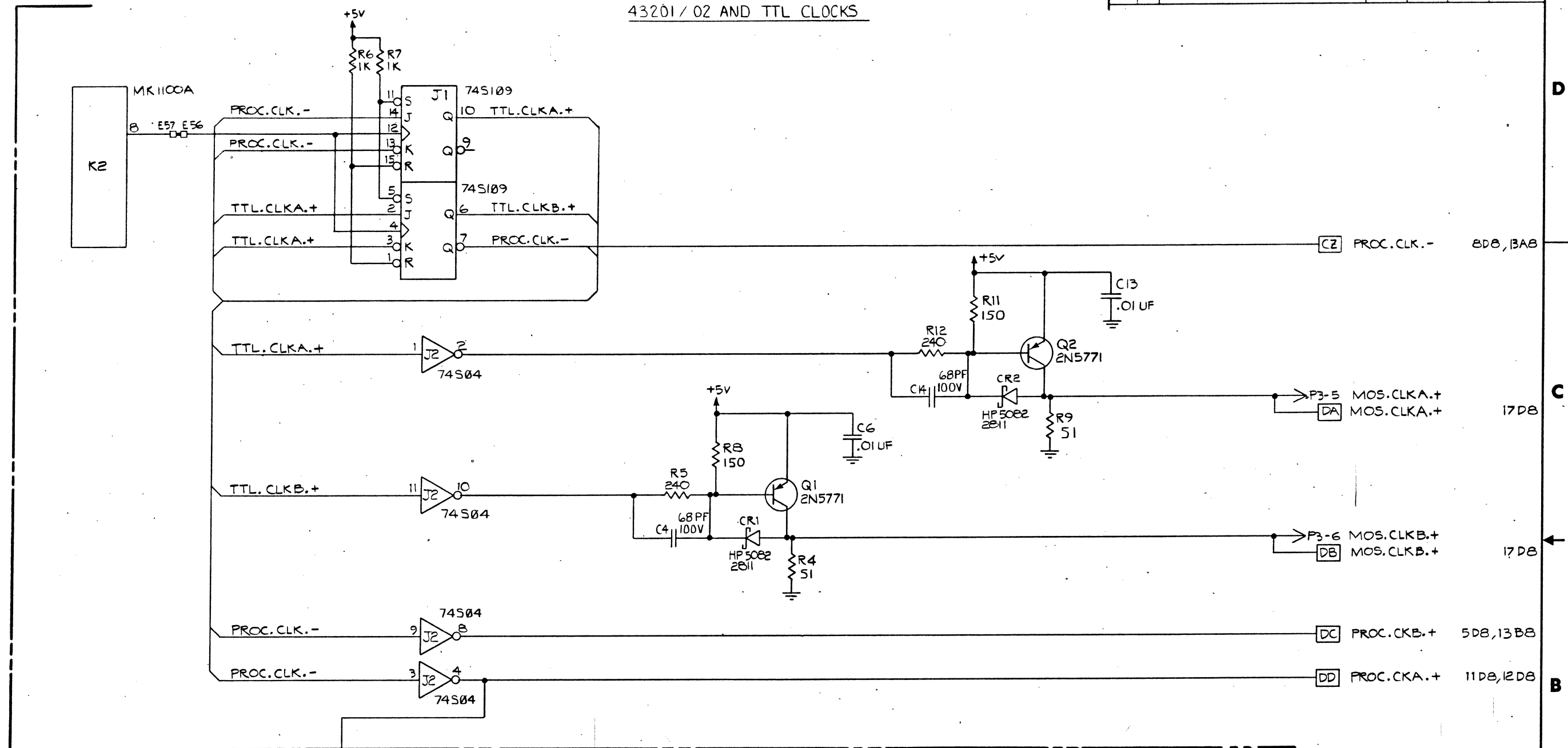
DWG NO. 172320		SH 16	REV A
ZONE	REV	DESCRIPTION	DFT
			CHK
			DATE
			APPROVED

D

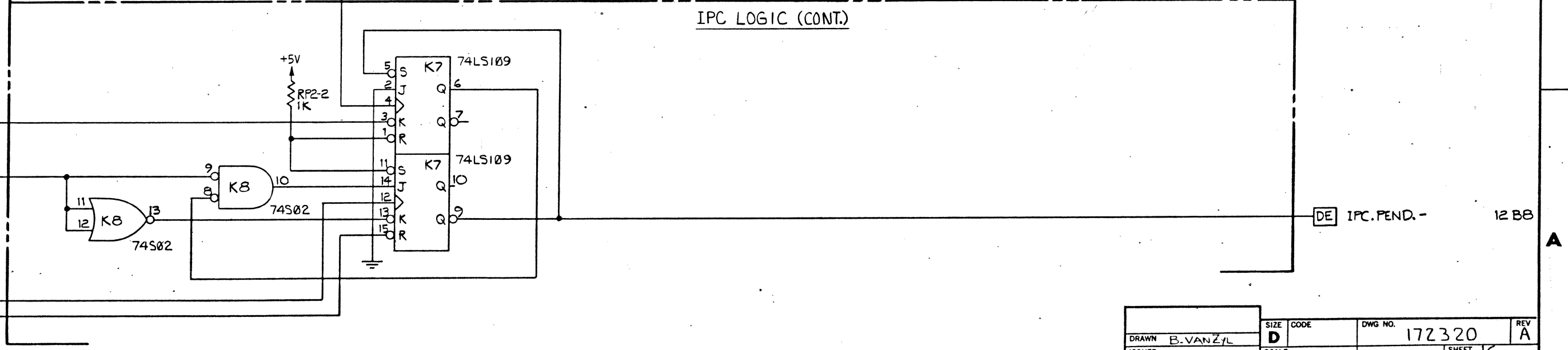
C

B

A



IPC LOGIC (CONT.)

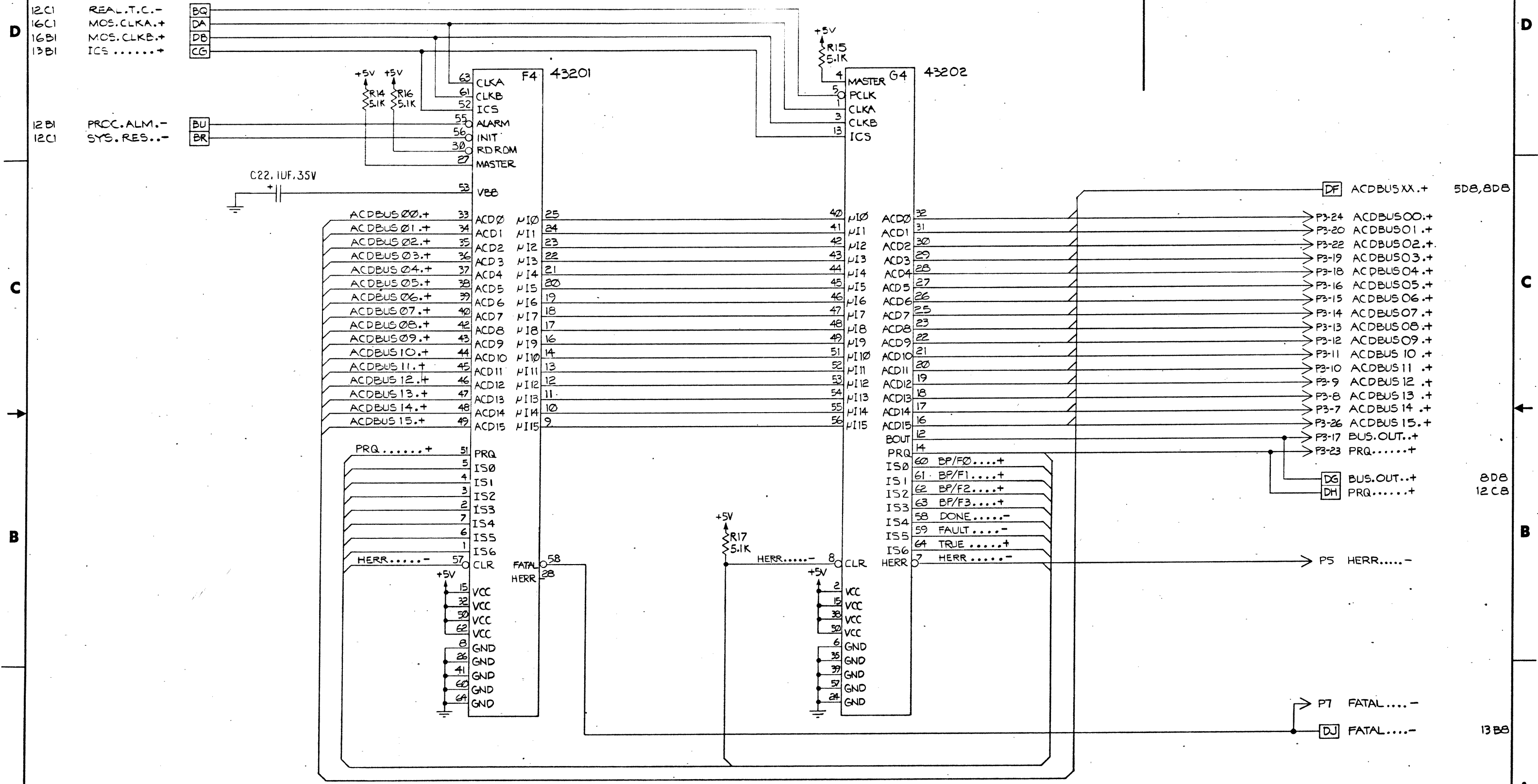


DRAWN B. VANZYL	SIZE D	CODE	DWG NO. 172320	REV A
ISSUED	SCALE		SHEET 16	

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43201/02 GDP

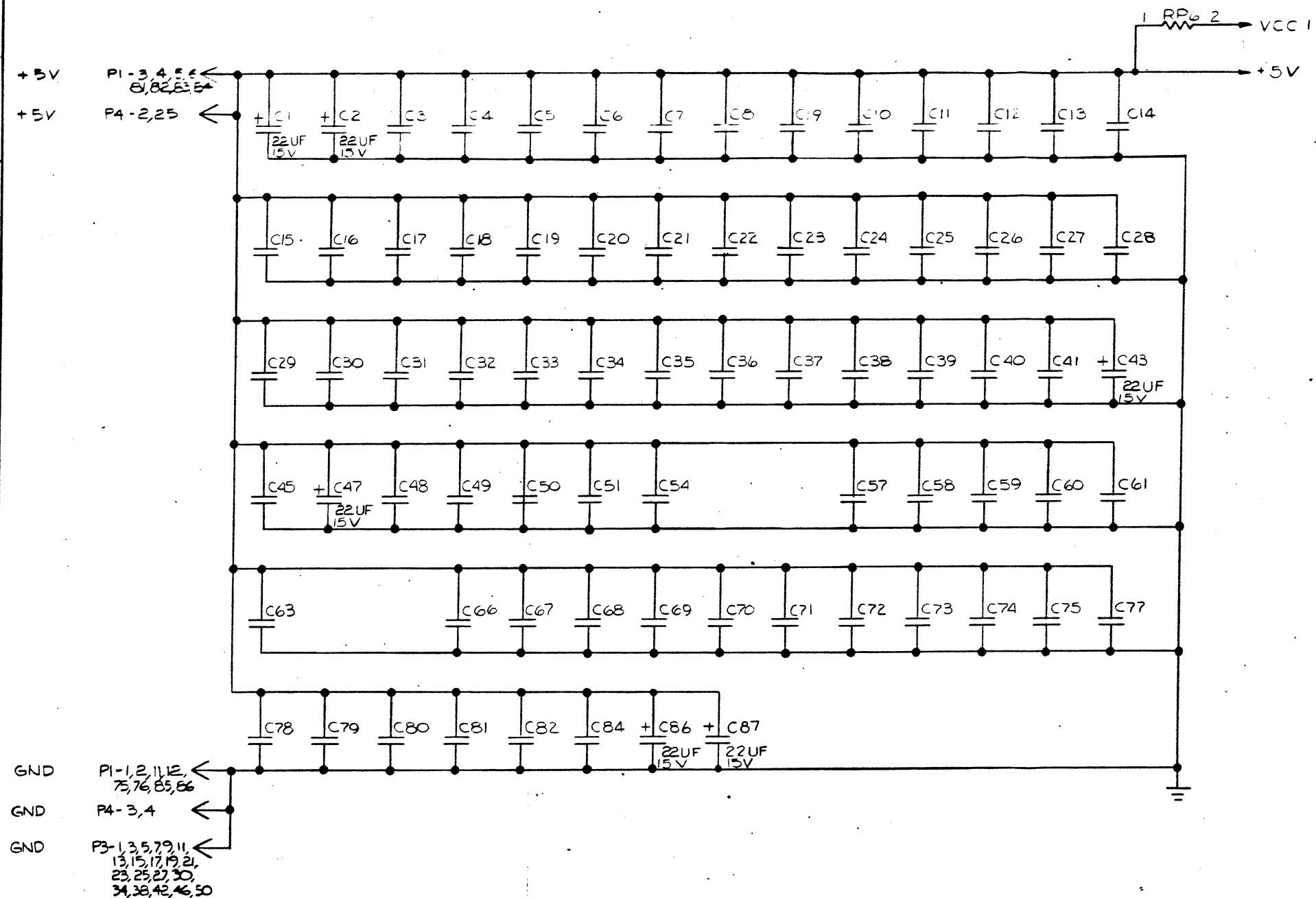
DWG NO.	172320	SH	17	REV	A	
REVISIONS						
ZONE	REV	DESCRIPTION	DFT	CHK	LATE	APPROVED



DRAWN	B. VANZYL	SIZE	D	CODE		DWG NO.	172320	REV	A
ISSUED		SCALE				SHEET	17		

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REV	DESCR	DFT	DATE	APPROVED
A	PER ECO 17-0214	BVZ	1/6/82	J.S.



REFERENCE DESIGNATION	DEVICE TYPE	GND PIN	+5V PIN	+12V PIN	-12V PIN	UNUSED OUTPUT PINS
A2	74S10	7	14			
J8	74LS38	7	14			J8-4,6,8
A4, A5, B3, E3, H9	74LS00	7	14			H9-3,6,8
E7	74LS02	7	14			E7
B2	74S04	7	14			
A7, G8, H8	74LS04	7	14			G8-4,10, H8-2,12
A3, B8, C5	74LS08	7	14			
A6	74LS10	7	14			
D3	74S11	7	14			
B9, C6	74S32	7	14			
B7	7438	7	14			
C3	74LS51	7	14			
C2	74S64	7	14			
E2	74S74	7	14			
A8	74LS74	7	14			
C7, C8, C9	74LS138	8	16			
C1	74S140	7	14			
B5	74LS151	8	16			
B4, D7	74LS174	8	16			B4-5, D7-15
B6	74LS175	8	16			
D1, F1, F3	74S240	10	20			D1-7,9
D8, D9, E8, G4, H4	74LS240	10	20			
G1, H1	74S280	7	14			
D2, G2, H2	74S374	10	20			
B1, E1, F2, F4, G3, H3	74LS374	10	20			
D4	74LS379	8	16			
J1, J2, J3, J4	74LS670	8	16			
C4	27S13C	8	16			
F6, F7	82S5A-5	7	26			
D6	82S9A	14	28			
E9, F8, F9	8287	10	20			
J6	43203	5,24,35,47	15,36,56			
E4	MK1100A	7	14			
RP1, RP2, RP4, RP5		8	1			
RP3, RP6, RP7, RP8		-	1			
A1	74LS164	7	14			

NOTES UNLESS OTHERWISE SPECIFIED
 1. CAPACITORS ARE .01UF, 50V.
 2. RESISTORS ARE IN OHMS, 1/4 W, ±5%.
 3. RESISTORS IN RP3, RP6, RP7, RP8 ARE 10KΩ, 1 1/2 W PER PACK, ±2%.
 4. RP1, RP2, RP4, RP5 DENOTE VALUES ARE IN OHMS, 2W PER PACK, ±5%.
 [E] THIS SIGNAL IS NOT FUNCTIONAL.

C87	C4244,46,52,53,62,76,83,85
CR2	
E88	
D51	
Q2	
F4	
RP8	
R7	
LAST USED	NOT USED
REFERENCE DESIGNATION	

ITEM NO.	PART NUMBER	DESCRIPTION
QUANTITY PER DASH NO.		
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. BREAK ALL SHARP EDGES. DO NOT SCALE DRAWING. TOLERANCES: ANGLES ± 2° XX ± .03 XXX ± .010 SURFACE FINISH 7		
SIGNATURE		DATE
DRN BYT DIRA/WA/MJA		1/7/82
CHK BY		1/7/82
ENGR APVD		1/7/82
APVD		
APVD		

365 BOWERS AVE
SANTA CLARA, CALIF. 95051

intel[®]

TITLE LOGIC DIAGRAM, PWA,
iSBC 432/602, IP

SIZE CODE 0100 DWG. NO. 172322 REV A

SCALE SHEET 1 OF 10

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REVISIONS		DATE	CHK	DFT	APPROVED
3	REV A				

- MB.AD.12 # - PI-32
- MB.AD.11 # - PI-30
- MB.AD.10 # - PI-28
- MB.AD.13 # - PI-34
- ACTIVATE. - AU

43203 WINDOW PAGE.SELECT

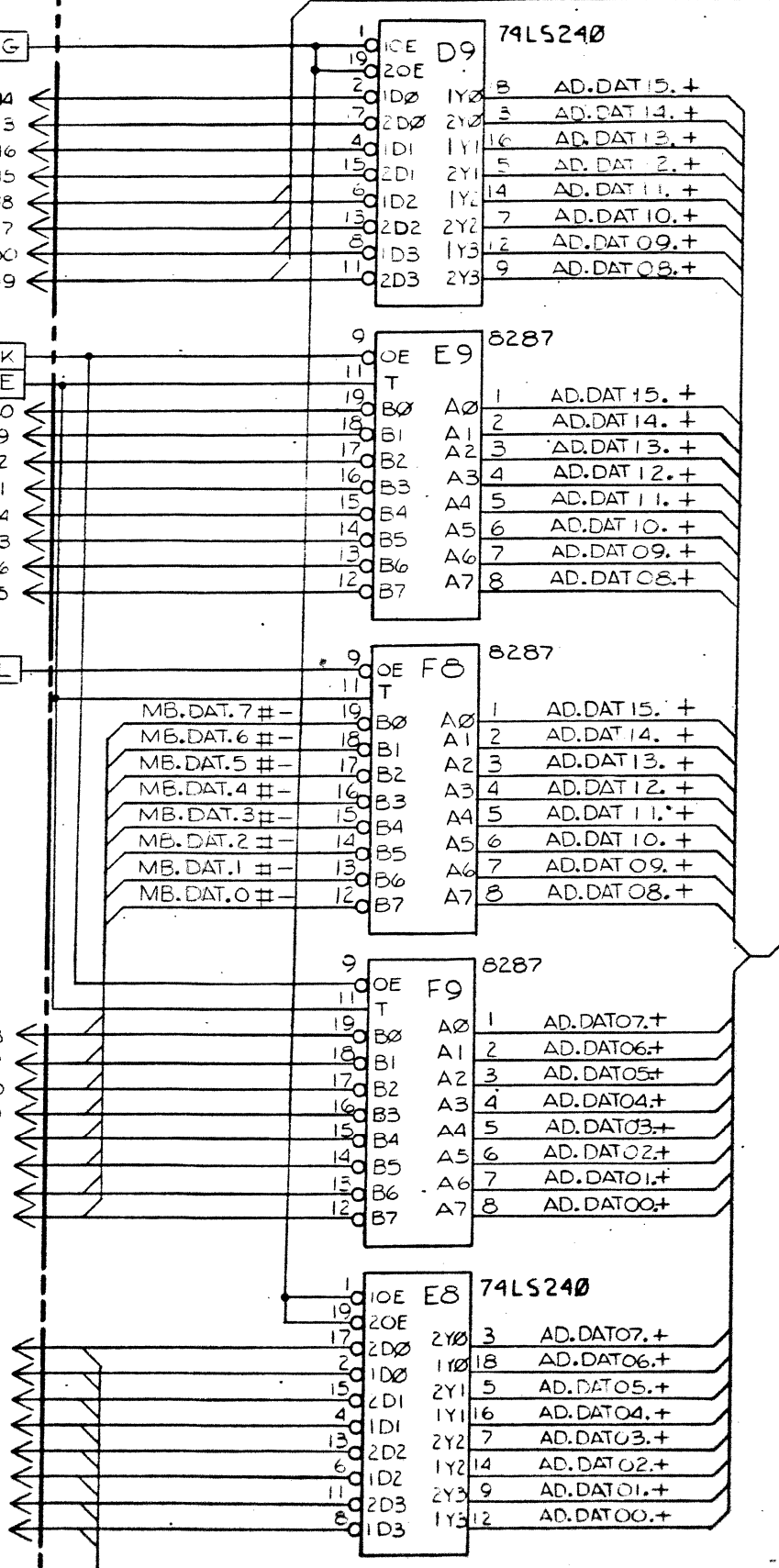
- MBUS.AEN. - G
- MB.ADR.F # - PI-44
- MB.ADR.E # - PI-43
- MB.ADR.D # - PI-46
- MB.ADR.C # - PI-45
- MB.ADR.B # - PI-48
- MB.ADR.A # - PI-47
- MB.ADR.9 # - PI-50
- MB.ADR.8 # - PI-49

- MBUS.DEN. - K
- MB.READ. + E
- MB.DAT.F # - PI-60
- MB.DAT.E # - PI-59
- MB.DAT.D # - PI-62
- MB.DAT.C # - PI-61
- MB.DAT.B # - PI-64
- MB.DAT.A # - PI-63
- MB.DAT.9 # - PI-66
- MB.DAT.8 # - PI-65

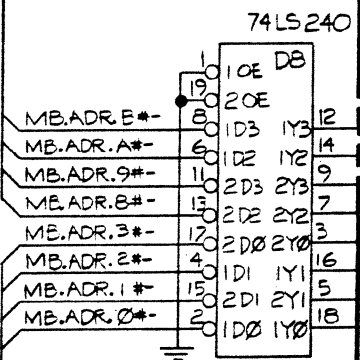
- MB.SWAP. - L

- MB.DAT.7 # - PI-68
- MB.DAT.6 # - PI-67
- MB.DAT.5 # - PI-70
- MB.DAT.4 # - PI-69
- MB.DAT.3 # - PI-72
- MB.DAT.2 # - PI-71
- MB.DAT.1 # - PI-74
- MB.DAT.0 # - PI-73

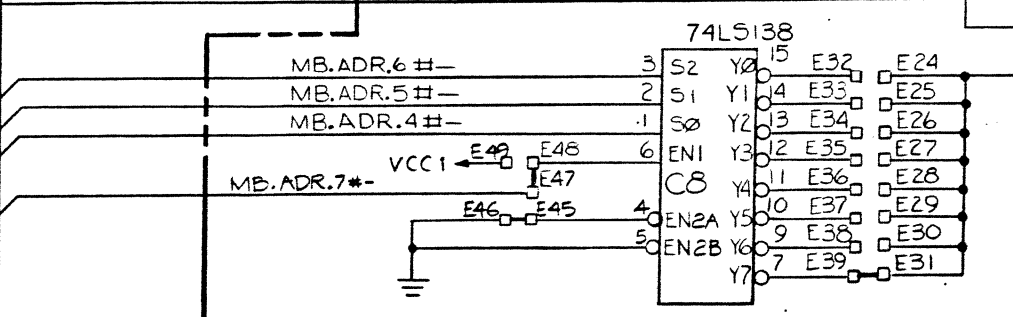
- MB.ADR.7 # - PI-52
- MB.ADR.6 # - PI-51
- MB.ADR.5 # - PI-54
- MB.ADR.4 # - PI-53
- MB.ADR.3 # - PI-56
- MB.ADR.2 # - PI-55
- MB.ADR.1 # - PI-58
- MB.ADR.0 # - PI-57



MULTIBUS ADDRESS/ DATA INTERFACE



I/O BASE ADDRESS SELECT

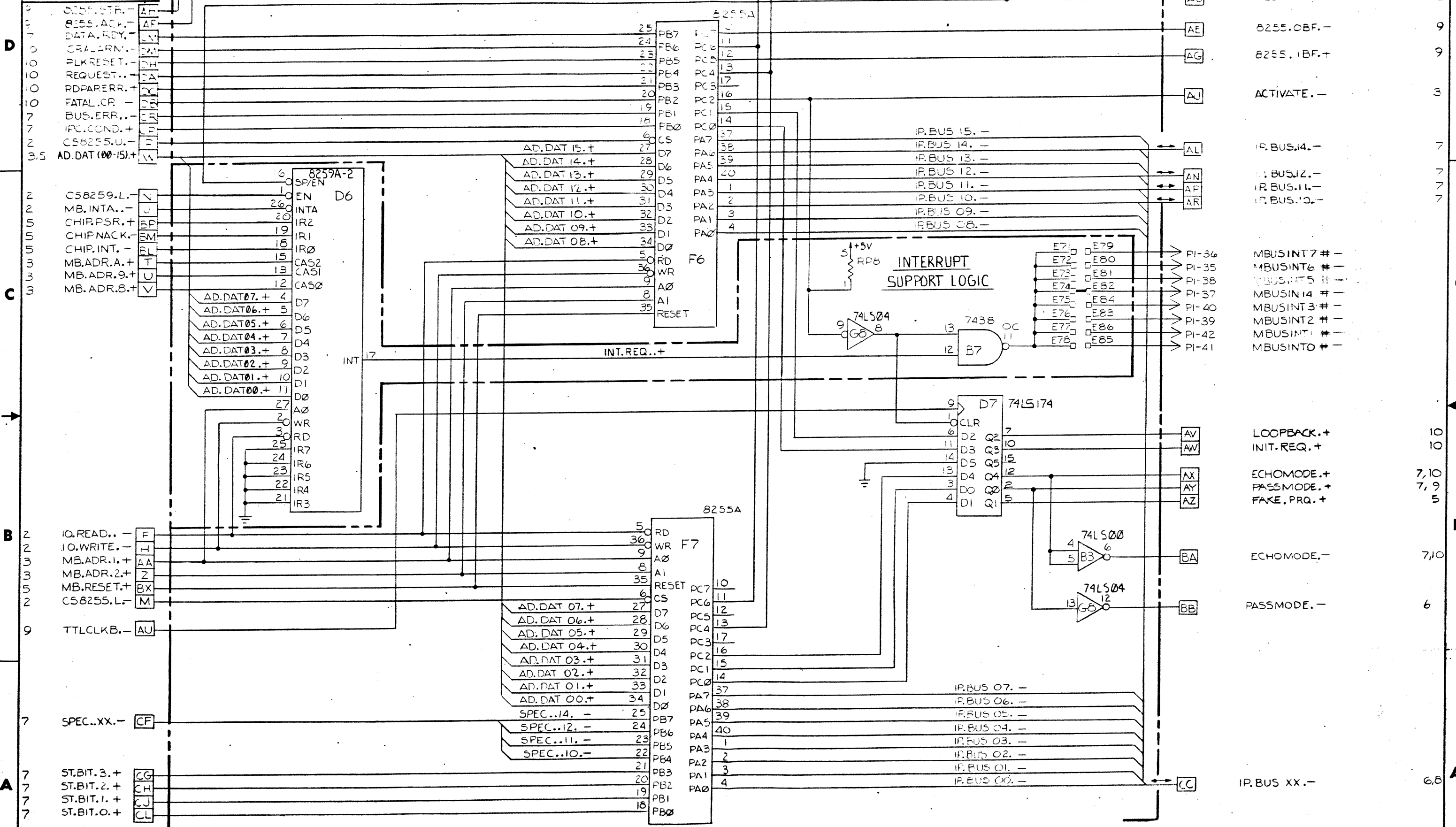


- MEMSEL. - S
- MB.ADR.A. + T
- MB.ADR.9. + U
- MB.ADR.8. + V
- MB.ADR.3. + Y
- MB.ADR.2. + Z
- MB.ADR.1. + AA
- MB.ADR.0. + AB
- AD.DAT(00-15). + W
- LOAD.SEL. - X

ECHO AND PASS MODE LOGIC

REV	DATE	APPROVED
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		

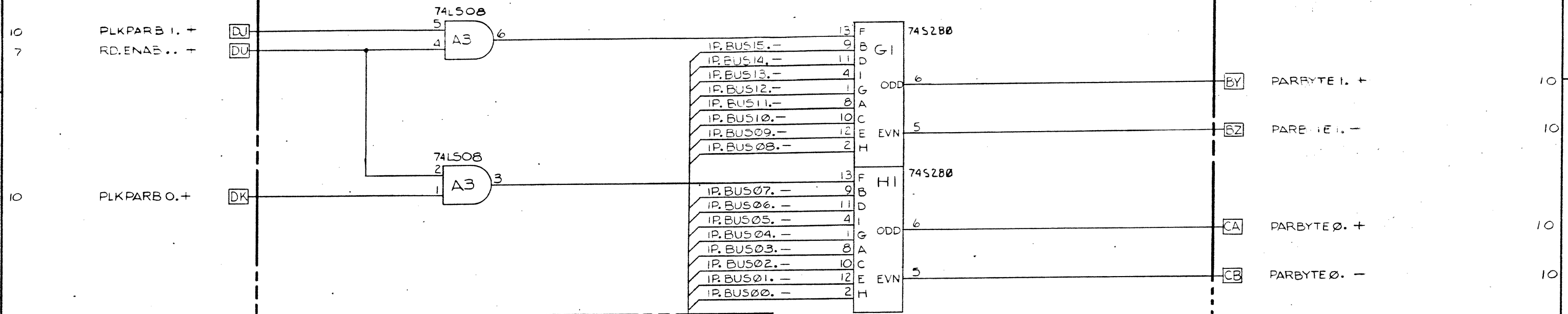
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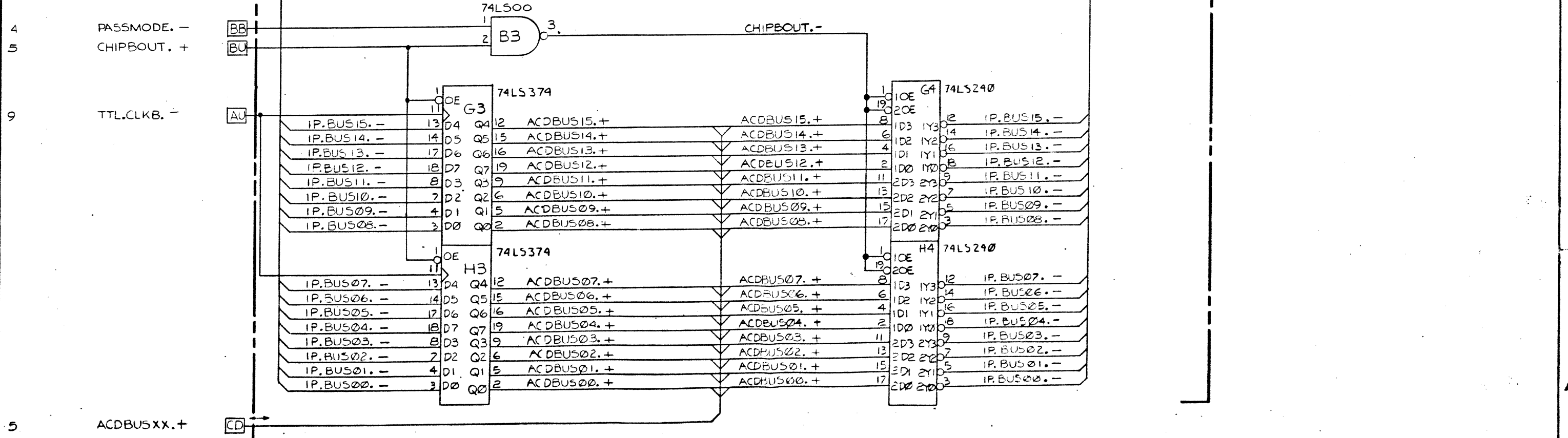
DRAWN	ISSUED	SIZE	CODE	DWG NO	REV
		D	0100	172322	A
		SCALE		SHEET 4	

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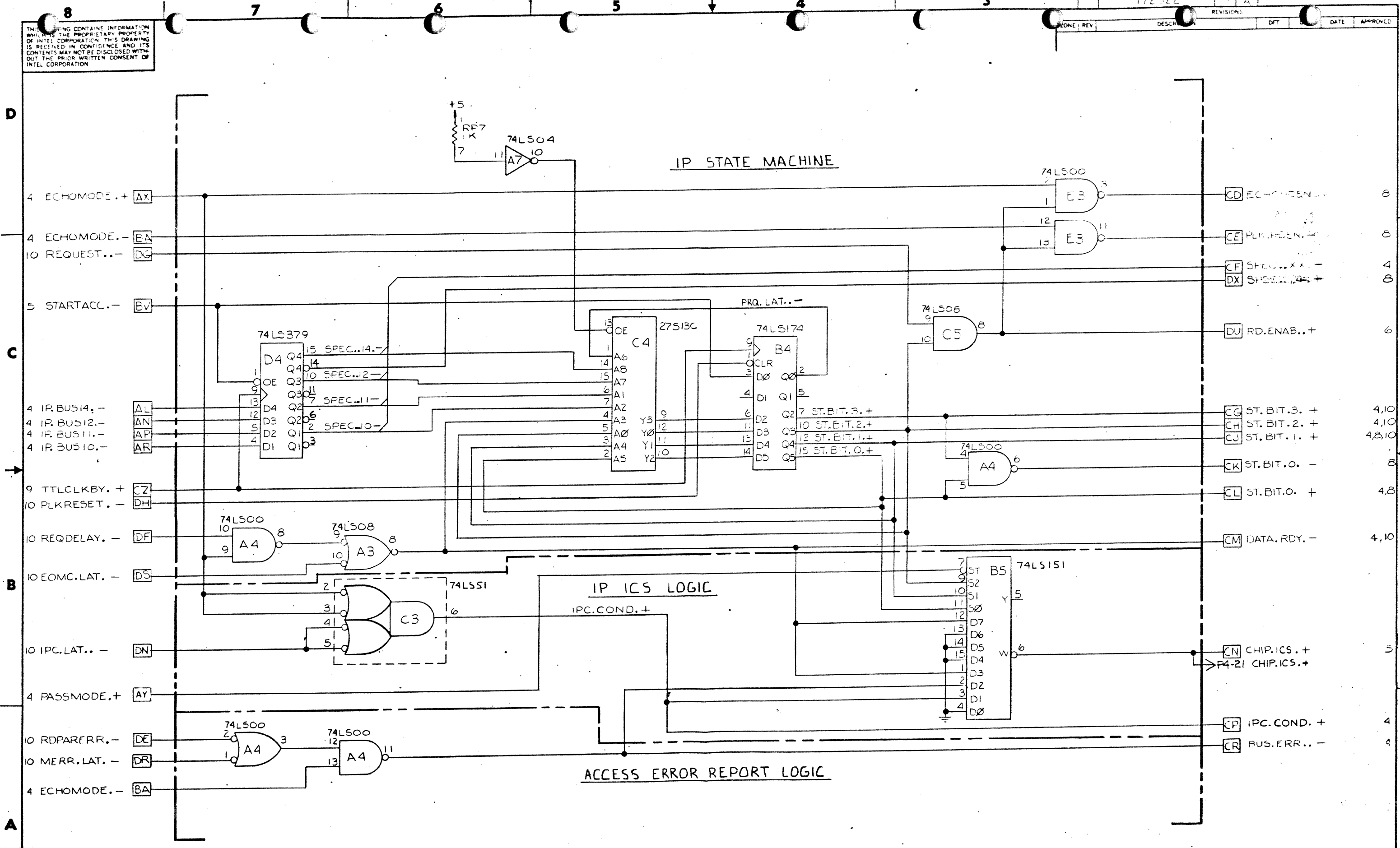
IP BUS PARITY GENERATORS/CHECKERS



ACD BUS TO IP BUS INTERFACE



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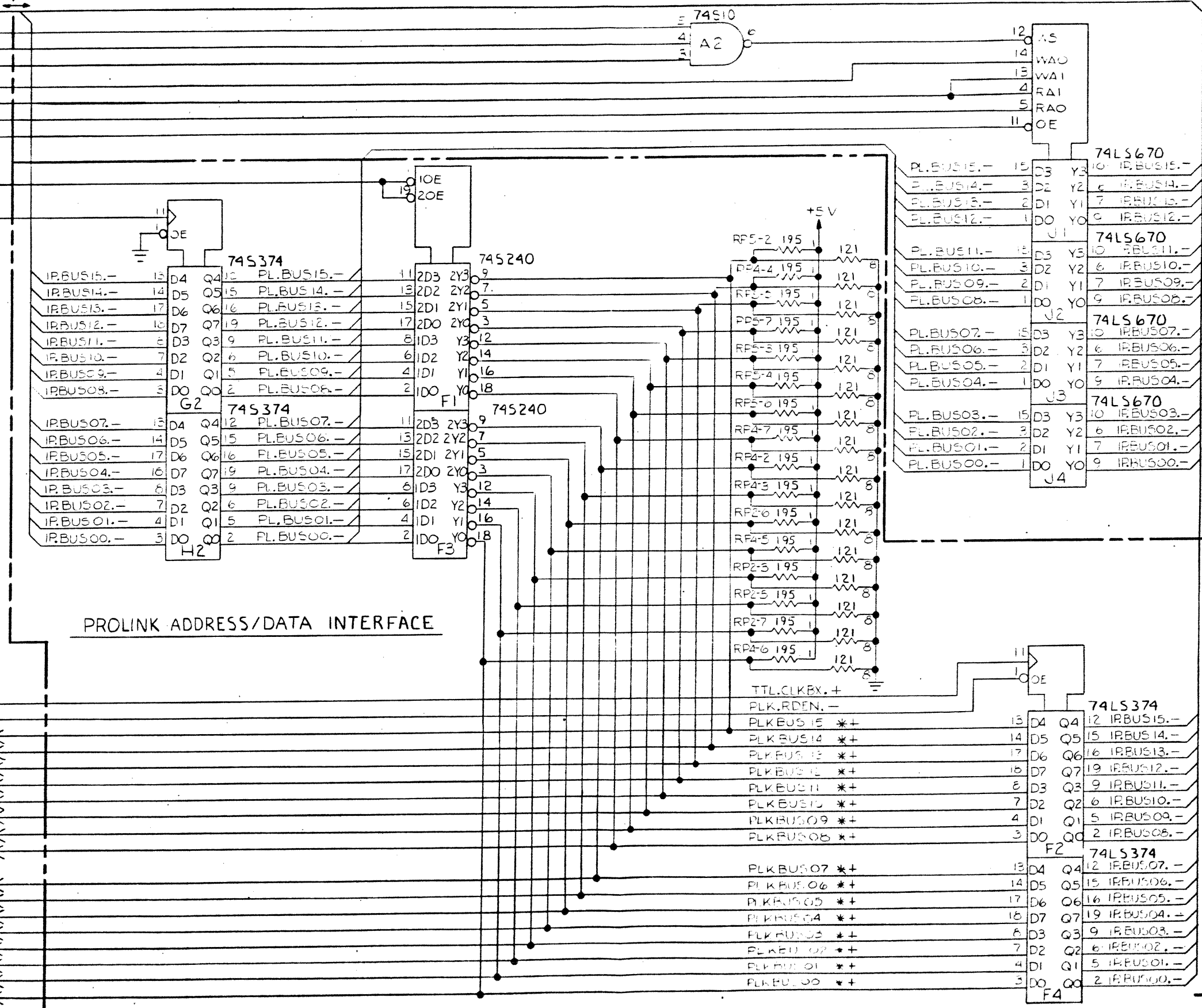
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ECHO MODE LOGIC

4 IP.BUSX.- CC
 0 REQUEST..+ DX
 7 SPEC..4.+ SX
 9 TTL.CLK.A.- CV
 7 ST.BIT.C.- CK
 7 ST.BIT.I.+ CU
 7 ST.BIT.O.+ CL
 7 ECHORDEN.- CD

10 REQUEST..- DG
 9 TTL CLKEX.+ CY

9 TTL CLK.BX.+ CY
 7 PLK.RDEN.- CE
 PLKBUS15 *+ P3-49
 PLKBUS14 *+ P3-40
 PLKBUS13 *+ P3-47
 PLKBUS12 *+ P3-45
 PLKBUS11 *+ P3-44
 PLKBUS10 *+ P3-43
 PLKBUS09 *+ P3-41
 PLKBUS08 *+ P3-40
 PLKBUS07 *+ P3-39
 PLKBUS06 *+ P3-37
 PLKBUS05 *+ P3-36
 PLKBUS04 *+ P3-35
 PLKBUS03 *+ P3-33
 PLKBUS02 *+ P3-32
 PLKBUS01 *+ P3-31
 PLKBUS00 *+ P3-29

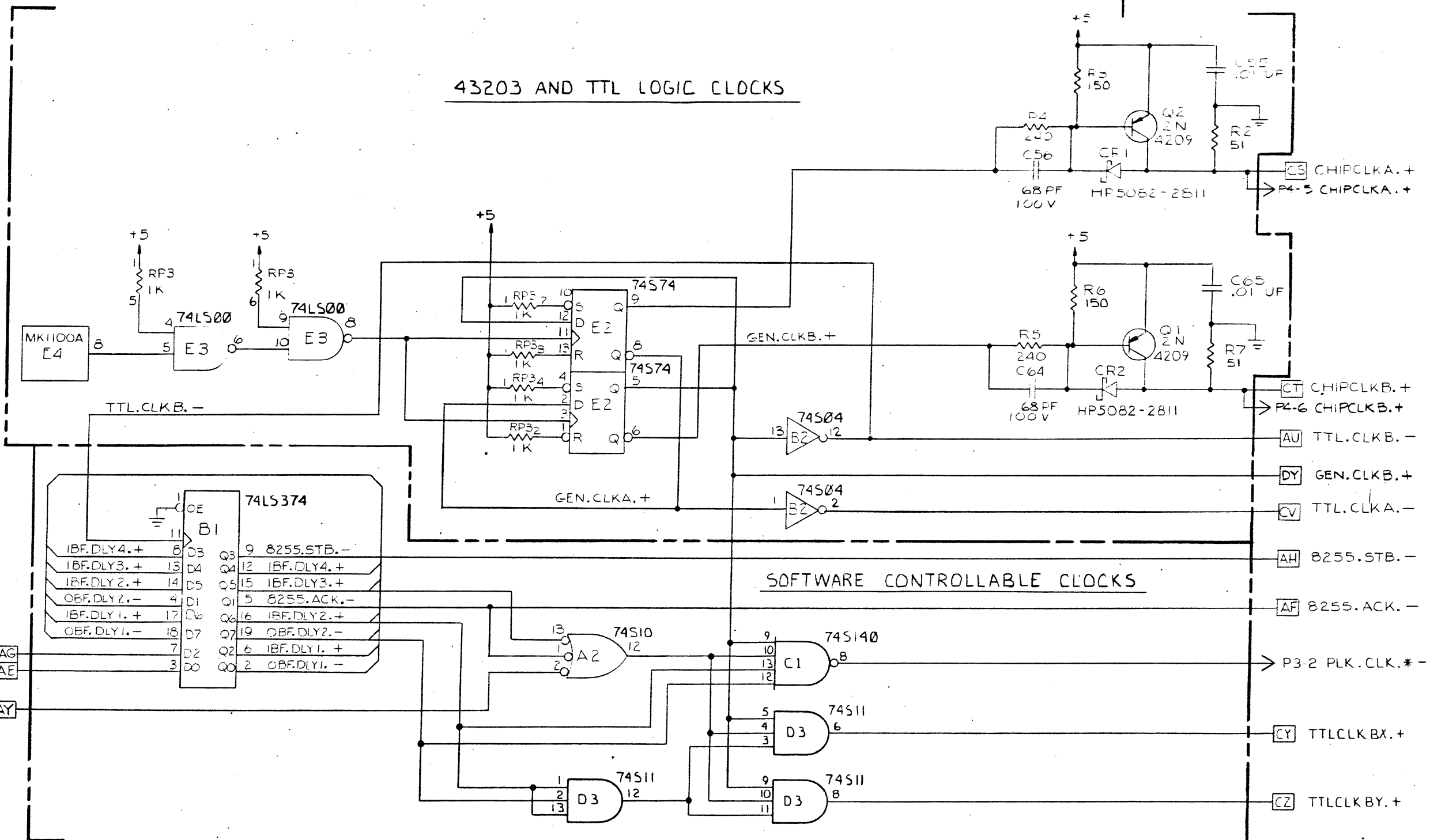


SIZE	CODE	DWG NO	REV
D	0100	172322	A
ISSUED	SCALE	SHEET	8

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DWG NO	172322	SH	REV	A		
ZONE	REV	DESCRIPTION	DFT	CHK	DATE	APPROVED

43203 AND TTL LOGIC CLOCKS



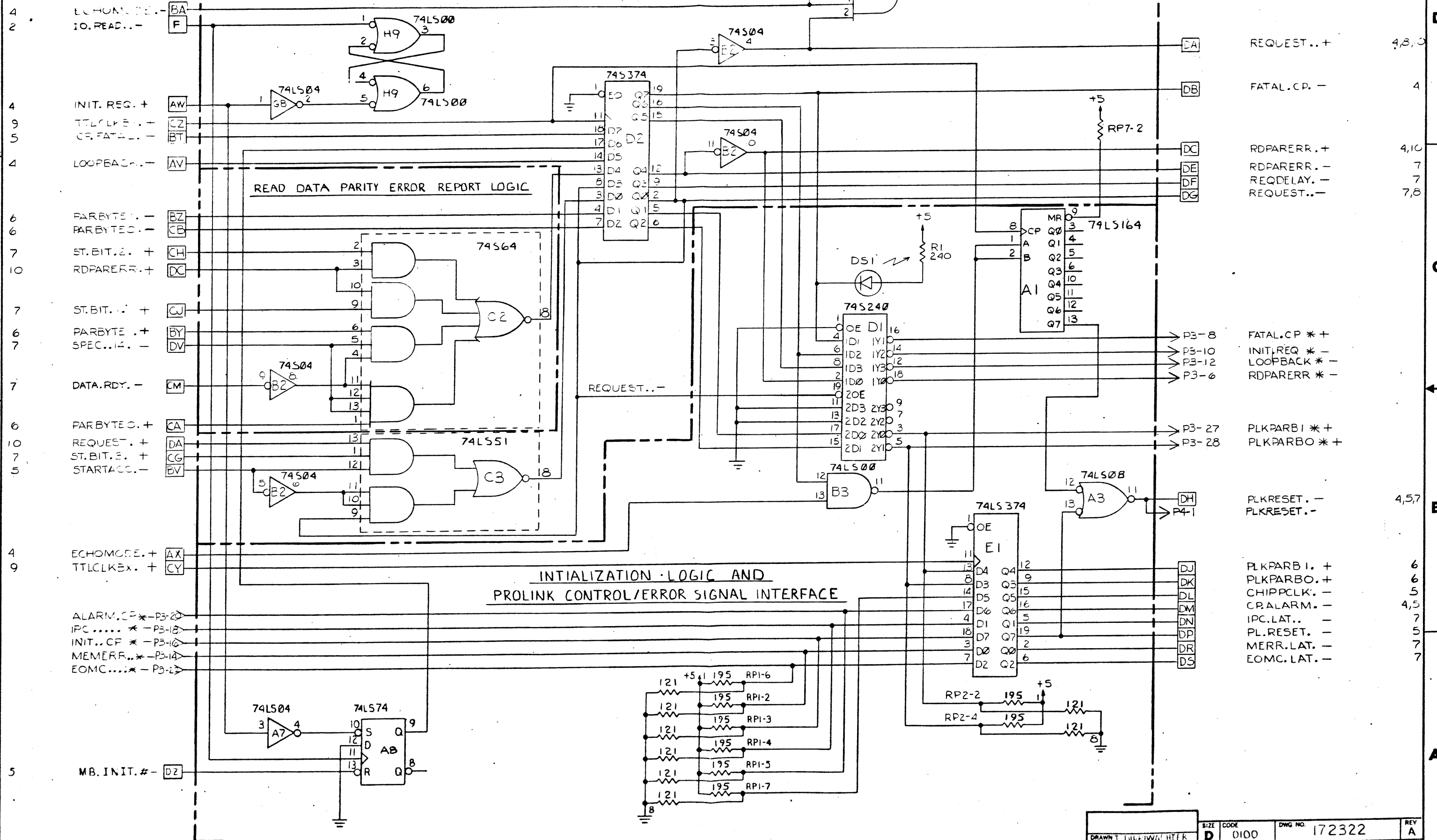
SIZE	D	CODE	0100	DWG NO	172322	REV	A
ISSUED		SCALE				SHLET	9

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PROCESSOR REQUEST LOGIC

READ DATA PARITY ERROR REPORT LOGIC

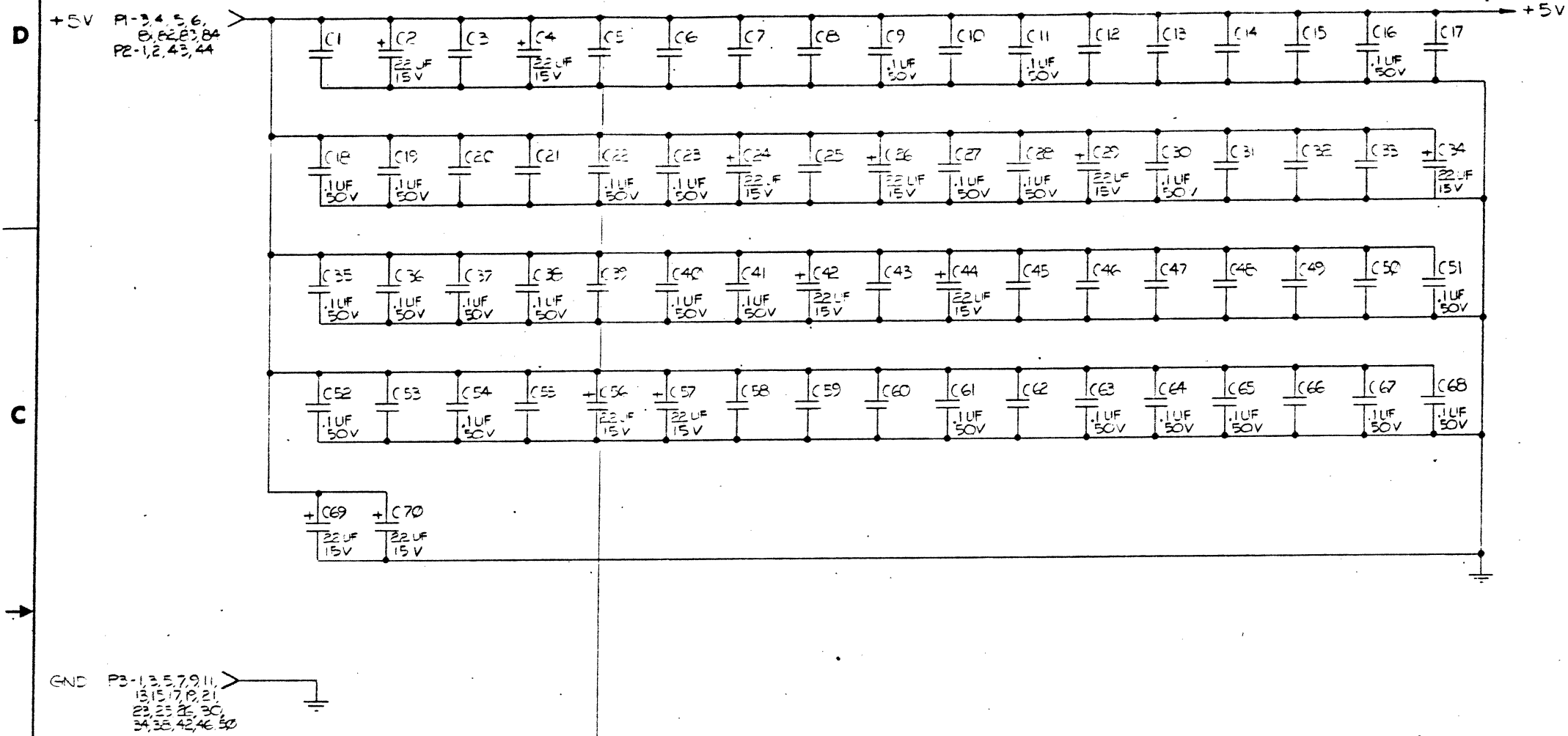
INITIALIZATION LOGIC AND PROLINK CONTROL/ERROR SIGNAL INTERFACE



4	REQUEST. *-	
4,8,9	REQUEST..+	
4	FATAL.CP. -	
4,10	RDPARERR.+	
7	RDPARERR.-	
7	REQDELAY. -	
7,8	REQUEST..-	
	FATAL.CP * +	
	INIT,REQ * -	
	LOOPBACK * -	
	RDPARERR * -	
	PLKPARB1 * +	
	PLKPARBO * +	
4,5,7	PLKRESET. -	
	PLKRESET.-	
6	PLKPARB1. +	
6	PLKPARBO.+	
5	CHIPCLK. -	
4,5	CR.ALARM. -	
7	IPC.LAT.. -	
5	PL.RESET. -	
7	MERR.LAT. -	
7	EOMC.LAT. -	

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REV	DESCR	DFT	DATE	APPROV
A	PER ECO 17-0213		7/5/62	



REFERENCE DESIGNATION	DEVICE TYPE	GND PIN	+5V PIN	UNUSED OUTPUT PINS
C2, E8, H8	74S00	7	14	CZ-11
F11, K5, K8	74S02	7	14	K5-3, 4, 10
K7, H1, H11, F12	74S04	7	14	H1-2, K7-6, F12-6, H1-8
H5	74LS04	7	14	
H7	74S10	7	14	H7-8
J7	74LS27	7	14	
H9	74S38	7	14	H9-3, 8, 11
K9, F10	74S51	7	14	F10-6
F9	74S74	7	14	
J3, J10	74LS109	8	16	
J8	74S112	8	16	
G10, H10	74LS138	8	16	
H6, K6	74S151	8	16	
G11	74LS151	8	16	
G3	74S153	8	16	
H4, K10	74S174	8	16	
G8	74S175	8	16	
J4	74LS175	8	16	
J11	74S240	10	20	
A2, A4, A11, B2, B4, B11, C11, D2, D4, D11, E10, E11, G12	74S241	10	20	
C3, E3, F3, J12	74LS244	10	20	
G7, J5, K12	74LS273	10	20	
E6, E7, G2	74S374	10	20	
A3, A10, A12, B3, B12, B12, C4, C10, C2, C3, D1, D2, E4, E9, E12, F4, H12, J9	74LS374	10	20	
G4	74LS377	10	20	
A5, A6, A7, AB, B5, B6, B7, B8, D3, D6, D7, D8	74LS670	8	16	
A9, B9, C5, C6, C7, C8, C9, D9, E5	25S10	8	16	
J6	27S21C	8	16	
F5, F6, F7, F8, G5, G6, H2, H3, K11	63S241	8	16	
RP1, RP2, RP3		8	16	
RP4, RP5, RP6, RP7		8	16	

NOTES UNLESS OTHERWISE SPECIFIED:
 1. CAPACITORS ARE .01 UF, 50V.
 2. RESISTORS IN RP1, RP2, RP3 ARE IN OHMS, 1.5W/PKG, ±2%.

ITEM NO.	PART NUMBER	DESCRIPTION
QUANTITY PER DASH NO		
PARTS LIST		
SIGNATURE	DATE	 3065 BOWERS AVE. SANTA CLARA, CALIF. 95051
DRN BY E. VAN ZYL	7-8-62	
CHK BY T. E. ...	7-8-62	
ENGR. APVD T. E. ...	7-8-62	
TITLE		LOGIC DIAGRAM, PWA, iSBC 432/603. TPL
SIZE	CODE	DWG NO. 172321
D		REV A
SCALE		SHEET 1 OF 15

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IPC LOGIC

DWG NO	172321	REV	A
ZONE	REV	DESCRIPTION	DFT
CHK	DATE	APPROVED	

D
C
B
A

D
C
B
A

PROC.ID2#+
PROC.ID1#+
PROC.ID0#+

P2-25
P2-29
P2-27

2 C1 IPC.W.OP.-
15 B1 DATA.S.D.-
6 A1 PADBUS02.+
6 A1 PADBUS01.+
6 A1 PADBUS00.+

G
DR
AX
AY
AZ

3 C1 BUS.MSTD.+
2 D1 IPC.R.OP.-

DB
F

2 D1 SYS.RST.-
2 D1 SYS.CLKB.+
2 D1 SYS.CLKA.+

C
A
B

3 C1 RES.REQD.-

U

Y PROC.ID2#+ 2A8
Z PROC.ID1#+ 2B8
AA PROC.ID0#+ 2B8

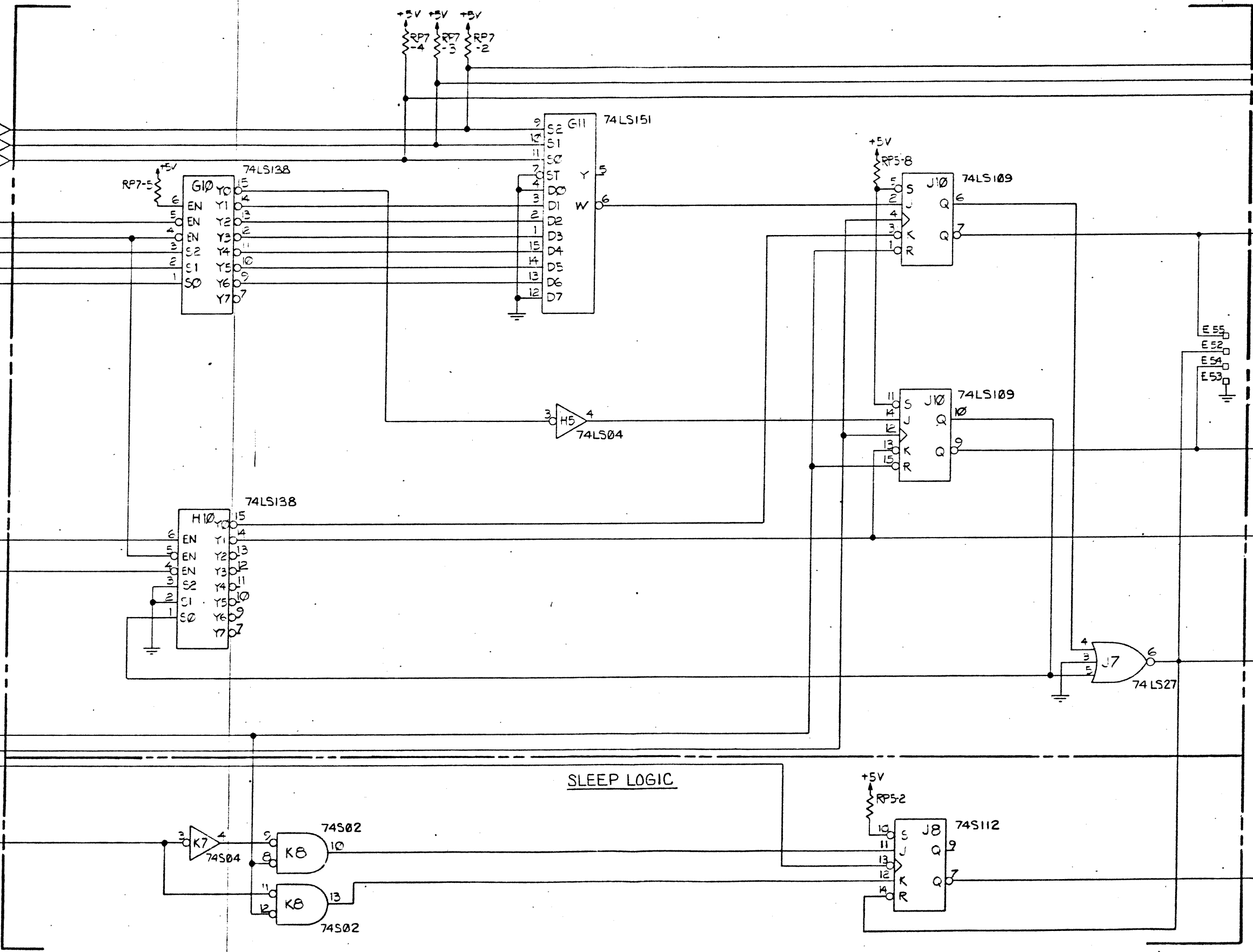
AB LCL.IPC... 2A8

AC GLBL.IPC.- 2A8

AD GLBL.RST.- 11A8

AE IPC.REQ... 11A8

AF SLEEP....- 14D8

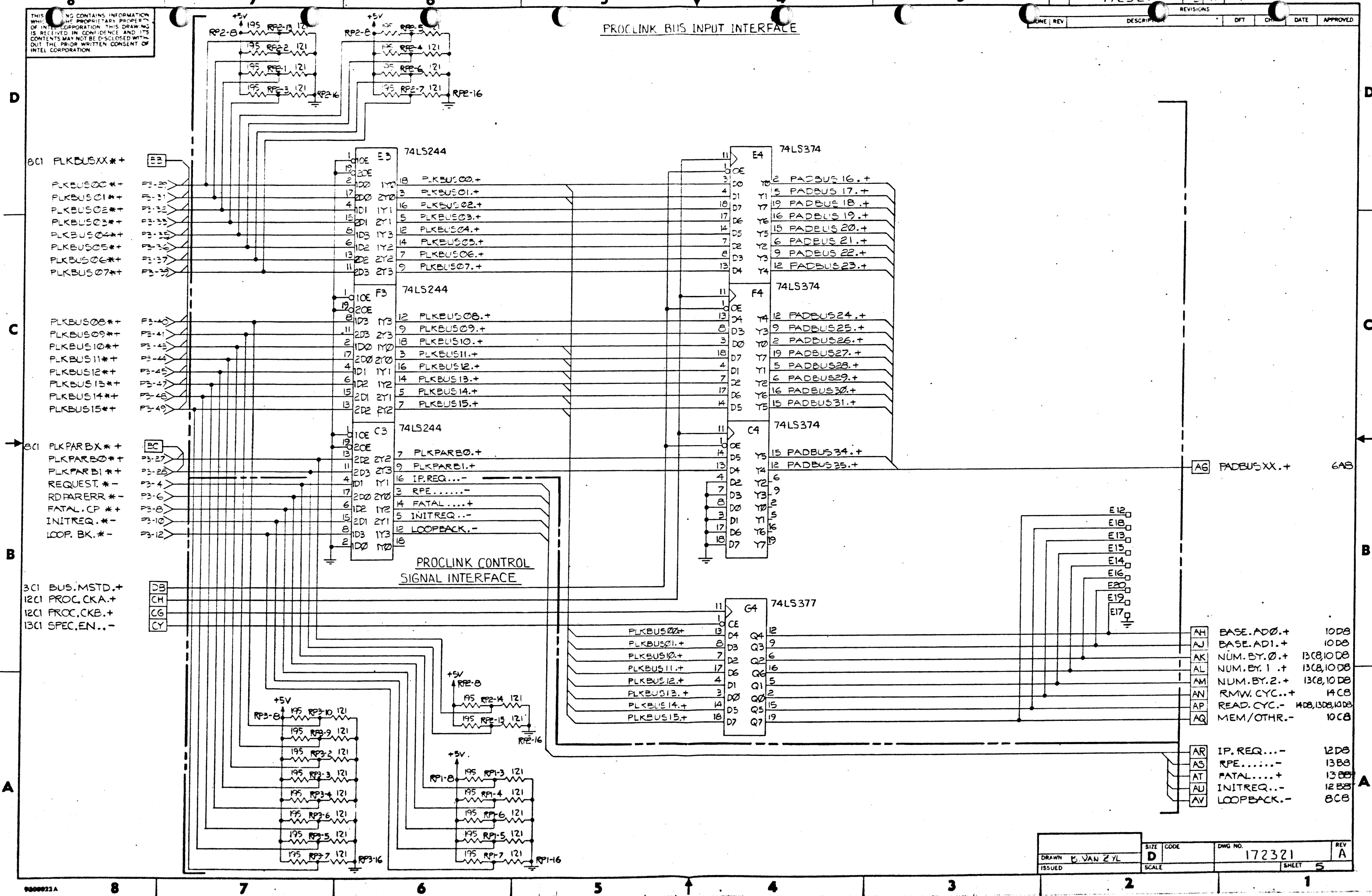


DRAWN	E. WILZ/L	SIZE	CODE	DWG NO	172321	REV	A
ISSUED		SCALE		SHEET	4		

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PROCLINK BUS INPUT INTERFACE

DWG NO	172321	REV	A
REVISIONS			
DATE			
APPROVED			



AH	BASE.AD0.+	10DB
AJ	BASE.AD1.+	10DB
AK	NUM.BY.0.+	13CB,10DB
AL	NUM.BY.1.+	13CB,10DB
AM	NUM.BY.2.+	13CB,10DB
AN	RMW.CYC..+	14CB
AP	READ.CYC.-	14DB,13DB,10DB
AQ	MEM/OTHR.-	10CB
AR	IP.REQ...-	12DB
AS	RPE.....-	13DB
AT	FATAL.....+	13DB
AU	INITREQ...-	12DB
AV	LOOPBACK.-	8CB

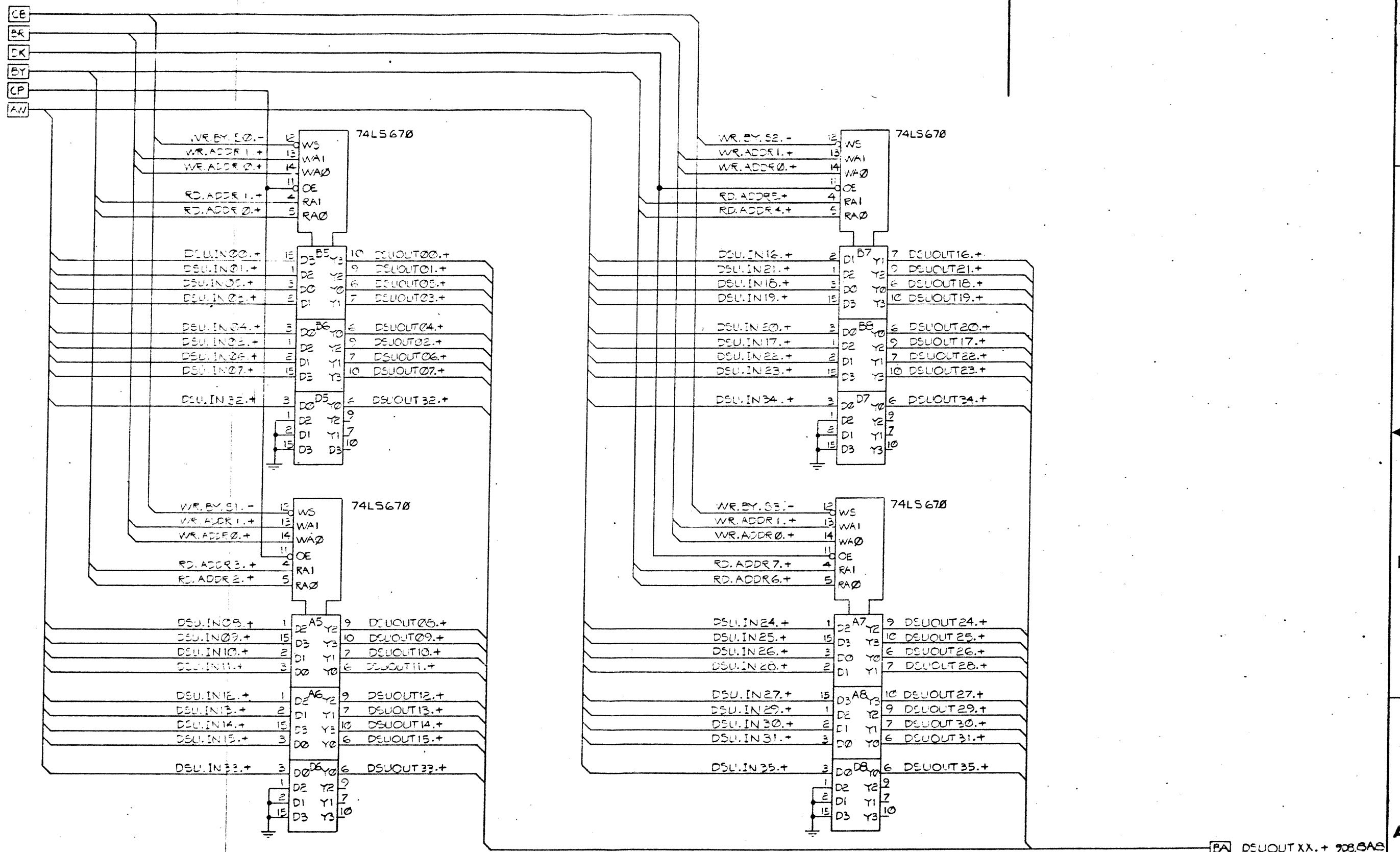
DRAWN	E. VAN ZYL	SIZE	D	CODE		DWG NO.	172321	REV	A
ISSUED		SCALE				SHEET	5		

DATA STORAGE UNIT

DWG NO	172321	REV	A
ZONE	REV	DESCRIPTION	DFT
CHK	DATE	APPROVED	

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- 11 C1 WR.BY.SX.-
- 10 C1 WR.ADDR1.+
- 15 C1 EN.DRSU.-
- 10 B1 RD.ADDR1.+
- 12 B1 DRSU.EN.-
- 6 D1 DSU.INXX.+



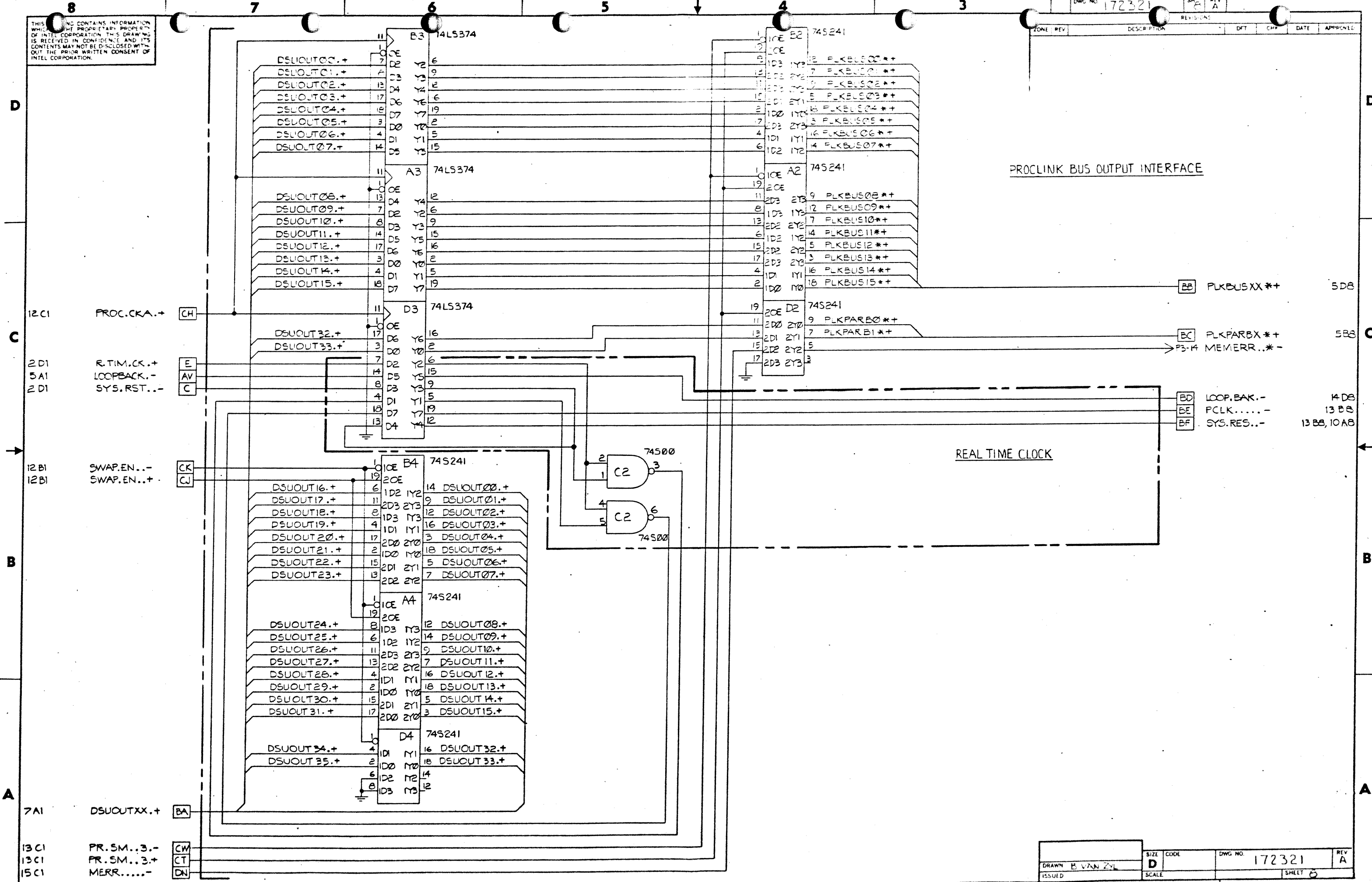
DSU.OUTXX.+ 908,0A8

DRAWN	E.VAN ZYL	SIZE	D	CODE		DWG NO.	172321	REV	A
ISSUED		SCALE				SHEET	7		

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DWG NO. 172321

ZONE	REV	DESCRIPTION	DFT	CHK	DATE	APPROVED



PROCLINK BUS OUTPUT INTERFACE

REAL TIME CLOCK

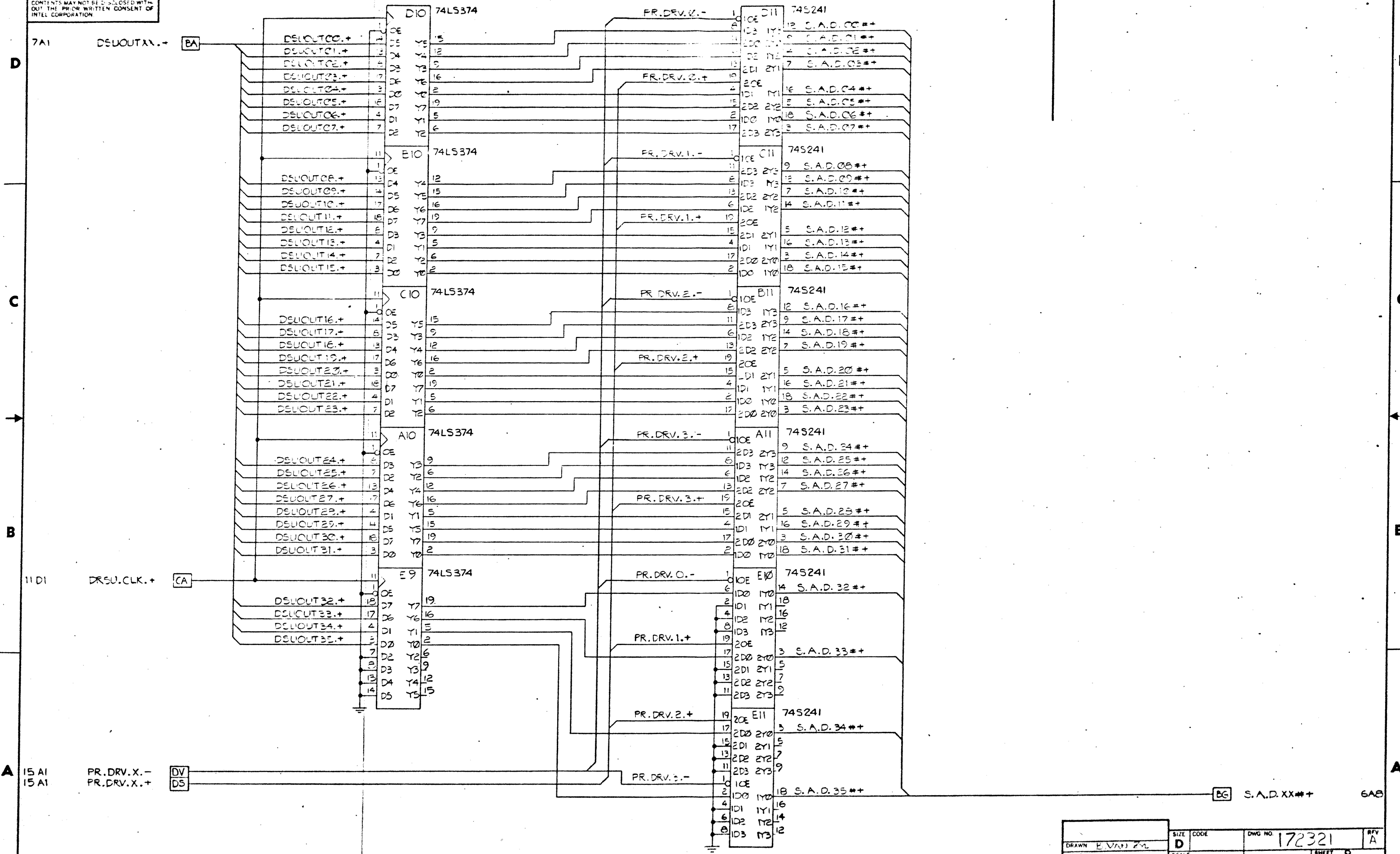
- BB PLKBUSXX** 5DB
- BC PLKPARBX** 5BB
- BD LOOP.BAK.- 14DB
- BE PCLK.....- 13BB
- BF SYS.RES.- 13BB, 10AB

DRAWN B. VAN ZYL	SIZE D	CODE	DWG NO. 172321	REV A
ISSUED	SCALE		SHEET 5	

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SAD BUS OUTPUT INTERFACE

DWG NO	172321	REV	A
REV		DATE	
DESCRIP		DFT	
APPROVED			



SIZE	CODE	DWG NO	172321	REV	A
ISSUED	SCALE	SHEET	9		

ZONE	REV	DESCRIPTION	DFT	CHK	DATE	APPROVED

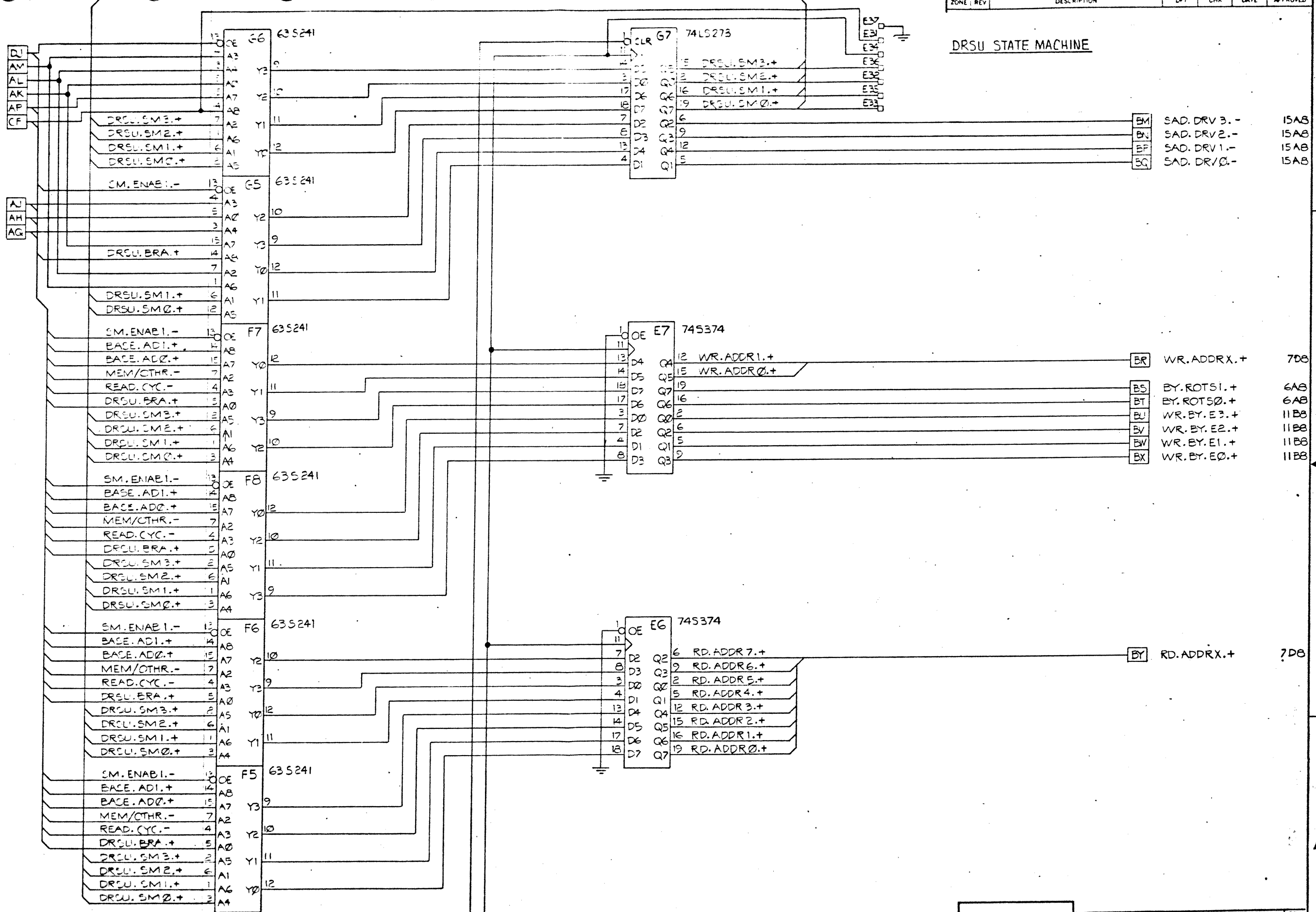
DRSU STATE MACHINE

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- 15 DI SM. ENABL. -
- 5 AI NUM. BY. 2. +
- 5 AI NUM. BY. 1. +
- 5 BI NUM. BY. 0. +
- 5 AI READ. CYC. -
- 12 CI DRSU. BRA. +

- 5 BI BASE. AD1. +
- 5 BI BASE. AD0. +
- 5 AI MEM/CTHR. -

- 8 CI SYS. RES. -
- 11 DI DRSU. CLK. +



- BM SAD. DRV 3. - 15AB
- BN SAD. DRV 2. - 15AB
- BP SAD. DRV 1. - 15AB
- BQ SAD. DRV 0. - 15AB

- BR WR. ADDR X. + 7DB
- BS BY. ROT S1. + 6AB
- BT BY. ROT S0. + 6AB
- BU WR. BY. E3. + 11B8
- BV WR. BY. E2. + 11B8
- BW WR. BY. E1. + 11B8
- BX WR. BY. E0. + 11B8

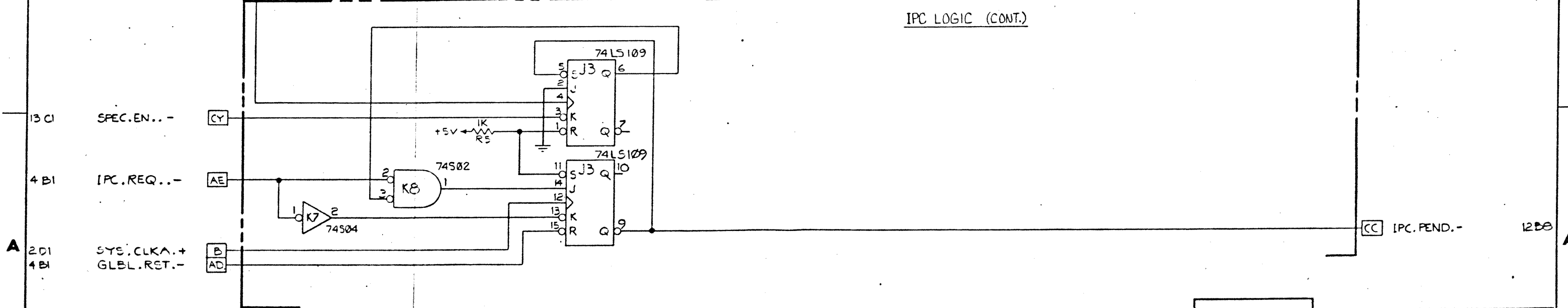
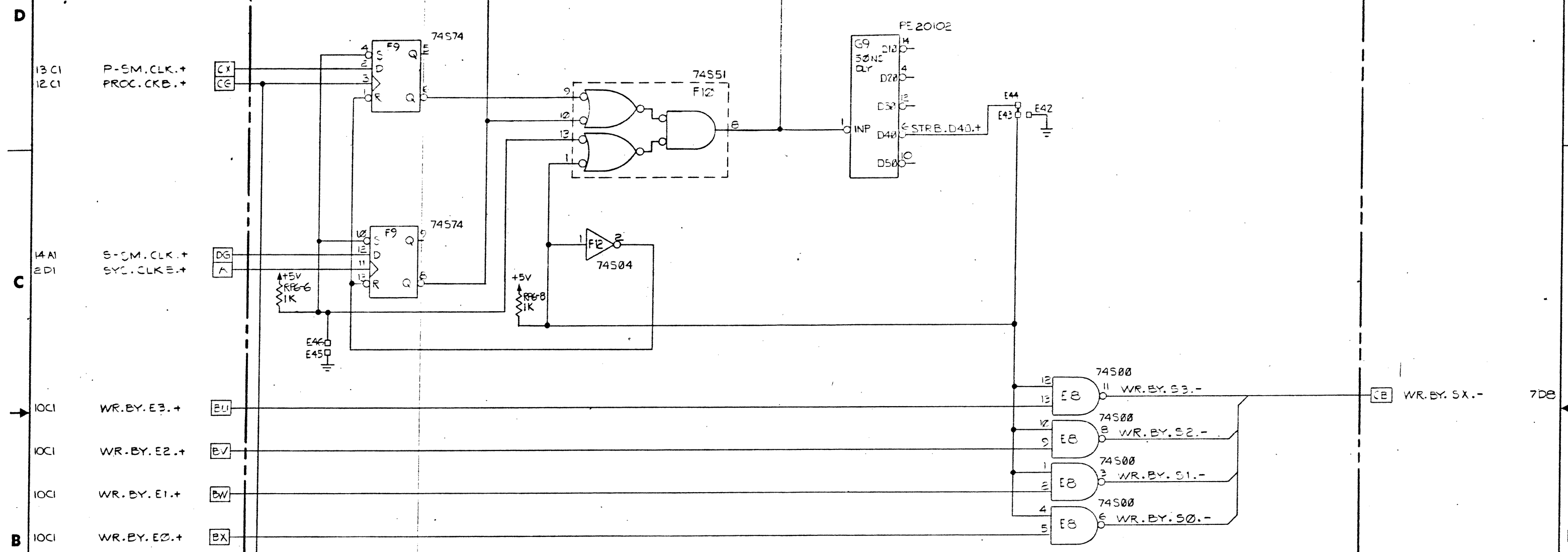
- BY RD. ADDR X. + 7DB

DRAWN	ISSUED	SIZE	CODE	DWG NO.	REV
T. V. J. P. V.		D		172321	A
		SCALE		SHEET	10

DRSJ CLOCK LOGIC

THIS DRAWING CONTAINS INFORMATION ON WHICH THE PROPRIETARY PROTECTION OF INTEL CORPORATION IS RELIED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION

REV.	DATE	APPROVED
1	172321	



- D 13 C1 P-SM.CLK.+
12 C1 PROC.CKB.+
- C 14 A1 S-SM.CLK.+
2 D1 SYN.CLKB.+
- B 10 C1 WR.BY.E3.+
10 C1 WR.BY.E2.+
10 C1 WR.BY.E1.+
10 C1 WR.BY.E0.+
- A 13 C1 SPEC.EN.-
4 B1 IPC.REQ.-
2 D1 4 B1 SYS.CLKA.+
4 B1 GLBL.REST.-

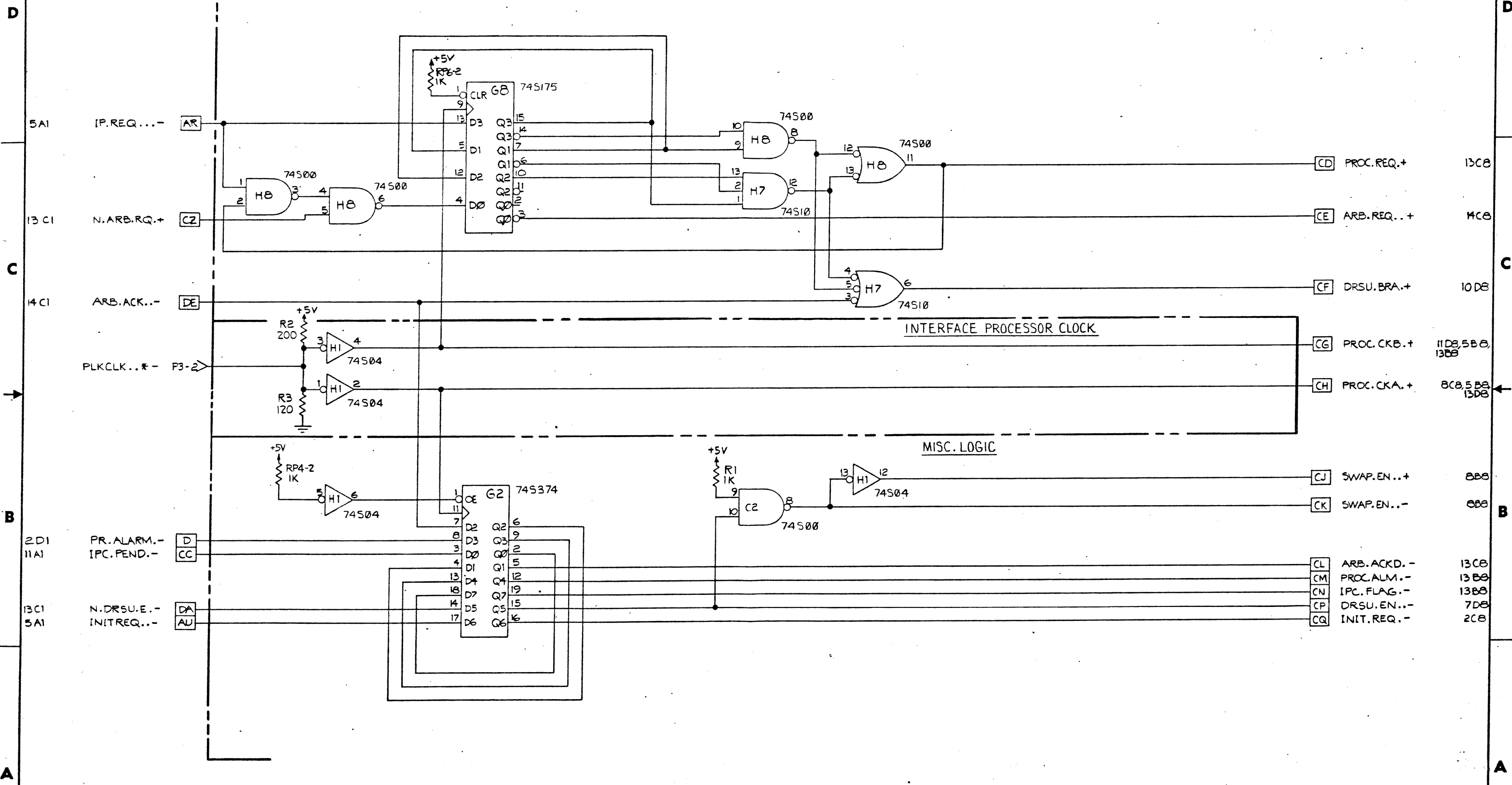
- B2 ERR CLR.- 15C8
- A DRSL CLK.+ 10A8,9B8
- CB WR.BY.SX.- 7D8
- CC IPC.PEND.- 12B8

DRAWN	SIZE	CODE	DWG NO	REV
ISSUED	D		172321	A
	SCALE		SHEET	1

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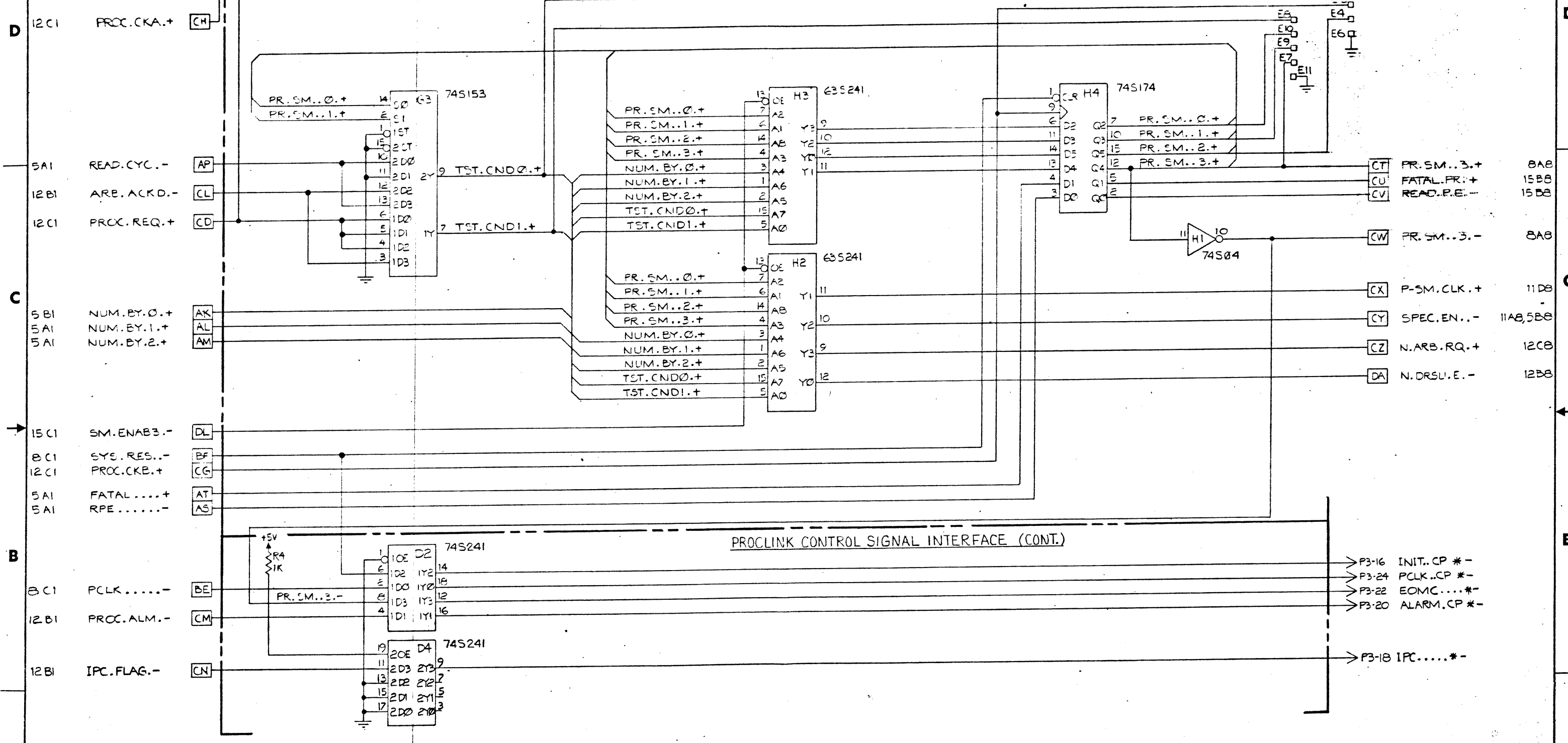
PROCESSOR REQUEST LOGIC

DWG NO 172321		SH 12	REV A
REVISIONS		DFT	CHK
ZONE	REV	DESCRIPTION	DATE
			APPROVAL



PROCESSOR STATE MACHINE

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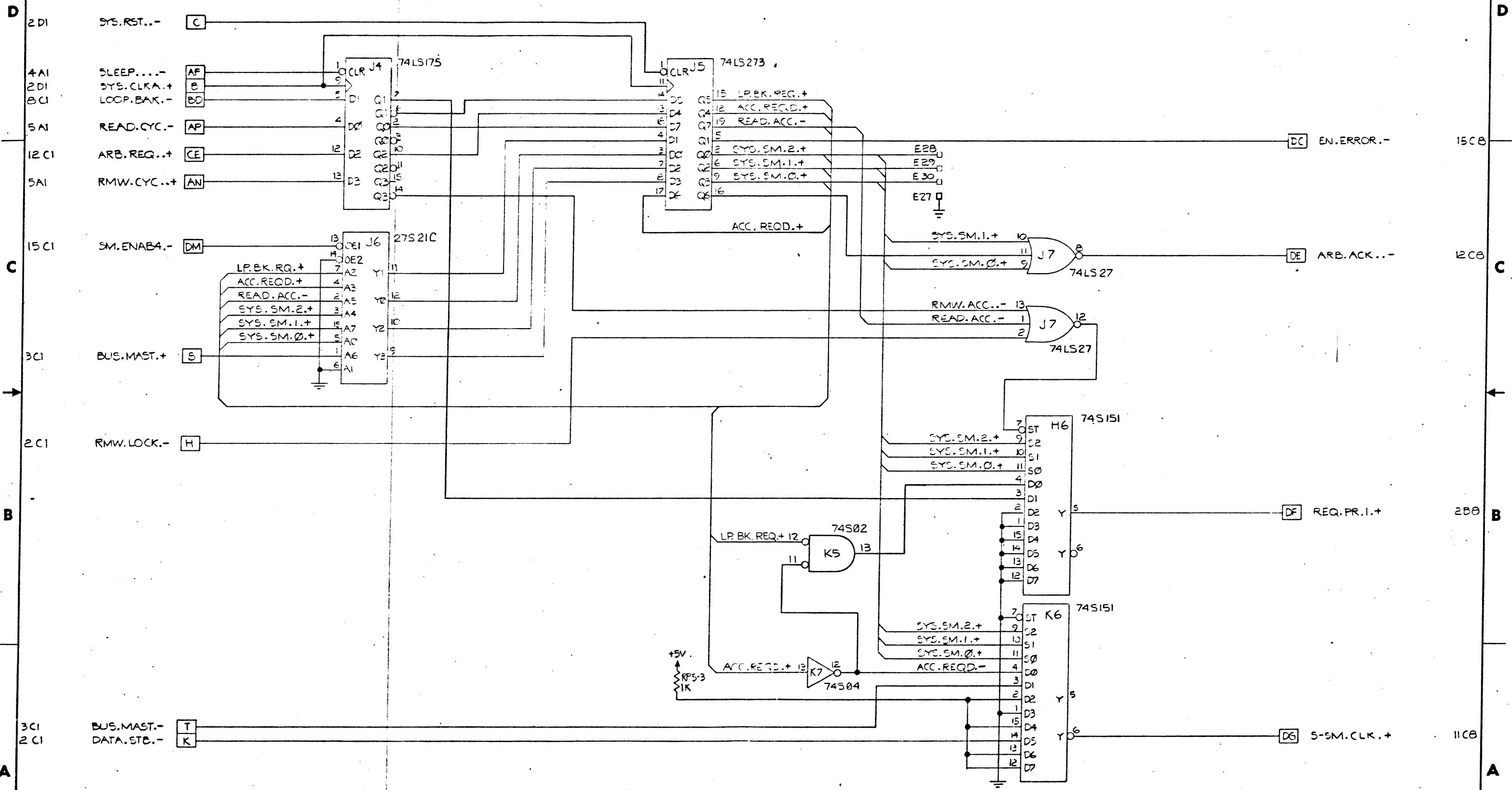


PROCLINK CONTROL SIGNAL INTERFACE (CONT.)

- > P3-16 INIT..CP *-
- > P3-24 PCLK..CP *-
- > P3-22 EOMC.....*-
- > P3-20 ALARM.CP *-
- > P3-18 IPC.....*-

SYS BUS STATE MACHINE

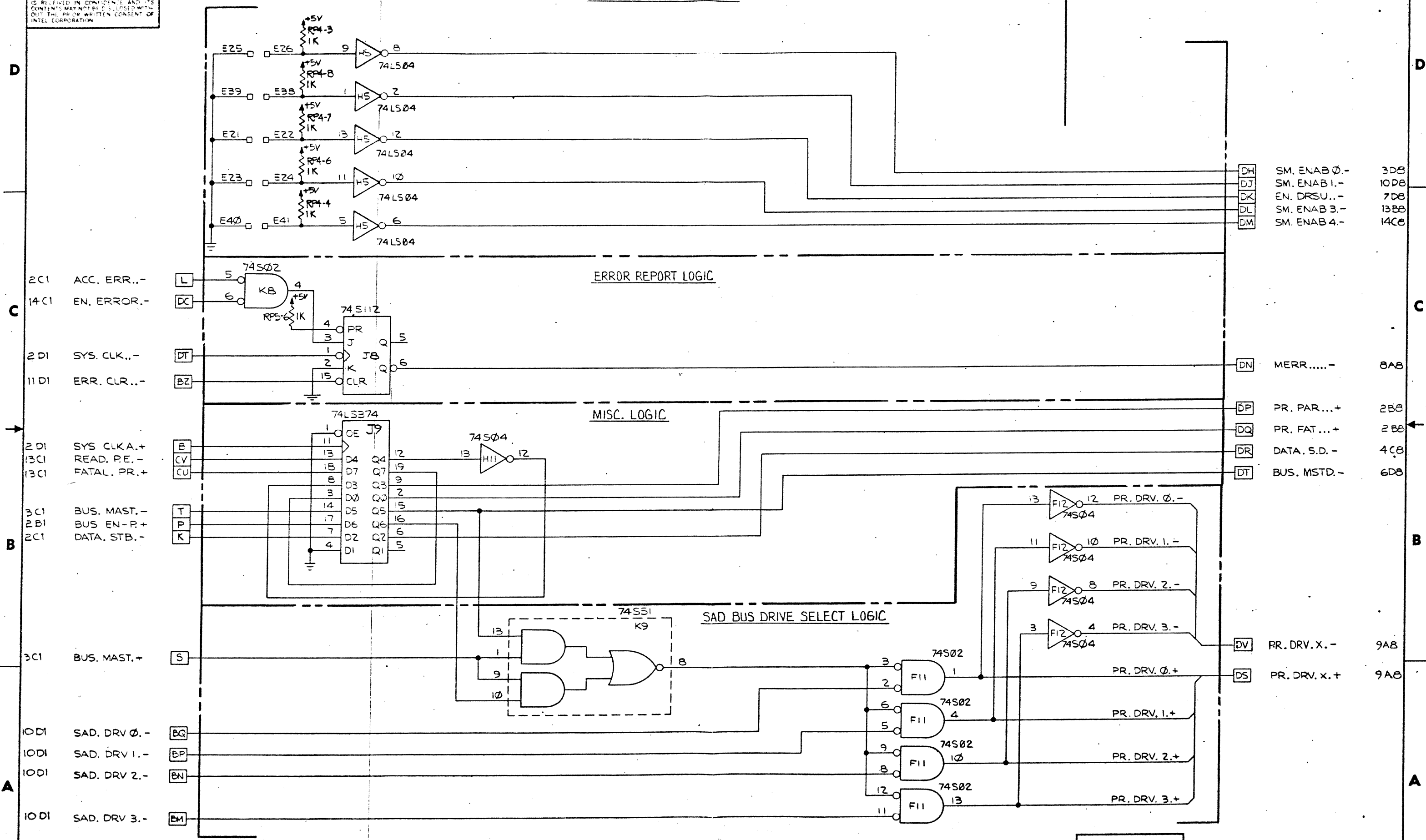
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TESTER CONTROL POINTS

DWG NO.	172321	REV	A
REV		DATE	
DESCRIPTION		CHK	
APPROVED			

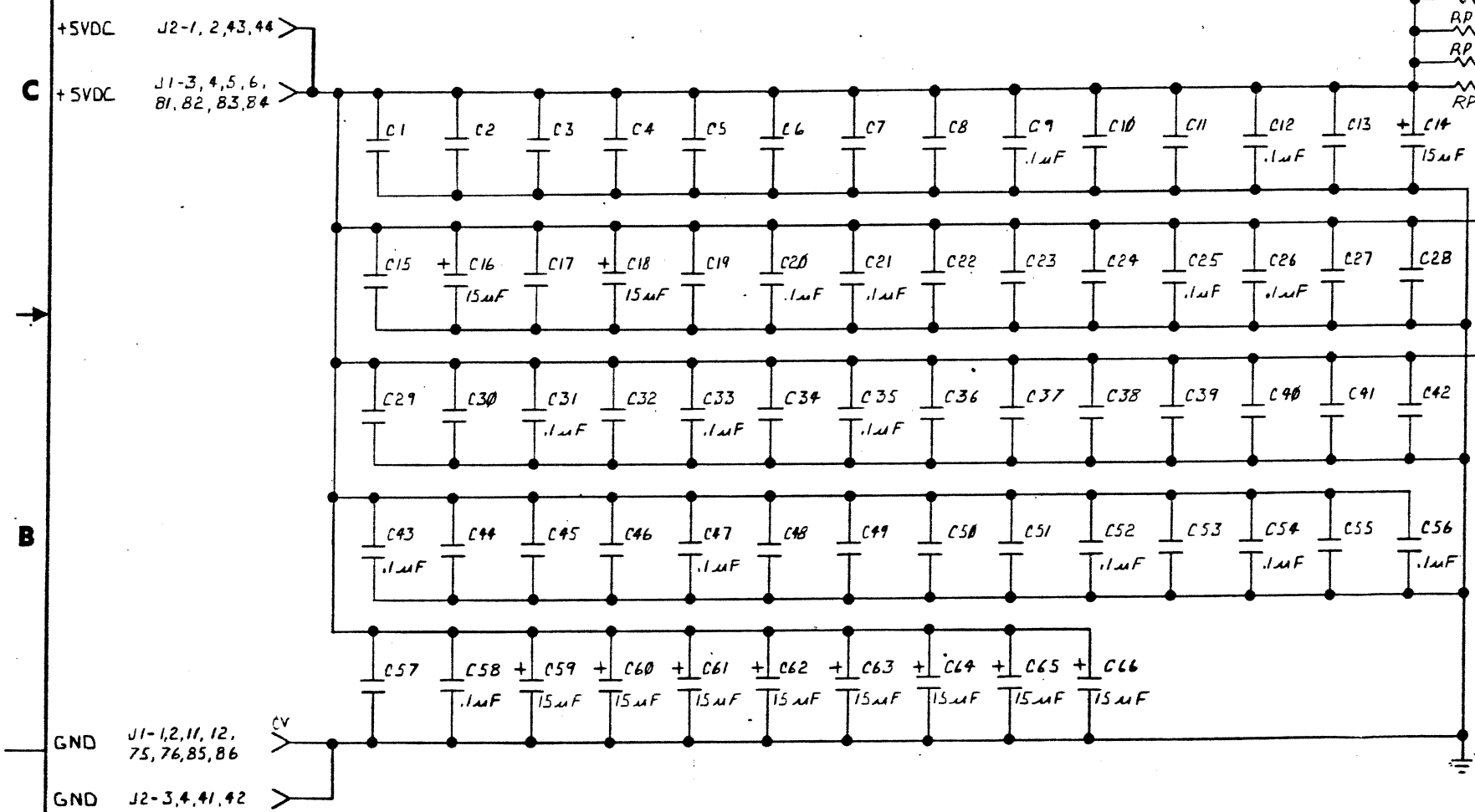


DRAWN	ISSUED	SCALE	SIZE	CODE	DWG NO.	172321	REV	A
						SHEET	15	

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REV		DESCRIPTION	DFT	CHK	DATE	APPROVED
A	PER ELO 17-0162				7/15/61	LS
B	PER ELO 17-0165				7/7/61	LS

RESISTOR	TERMINAL	VCC	TERMINAL	TERMINAL
RP3-8	A	VCC.A....+		2,7,13
RP3-5	E	VCC.B....+		3
RP3-4	C	VCC.C....+		3
R1	U	VCC.D....+		4
RP1-3	E	VCC.E....+		5
RP8-8	F	VCC.F....+		6,7,9,10,11
RP8-4	G	VCC.G....+		6,7,11
RP8-2	H	VCC.H....+		7
RP8-3	J	VCC.I....+		10
RP4-2	K	VCC.K....+		7
RP6-7	L	VCC.L....+		7
RP5-3	M	VCC.M....+		8,9
RP3-2	N	VCC.N....+		10
RP4-5	O	VCC.P....+		10
RP4-3	P	VCC.R....+		12
RP7-6	Q	VCC.S....+		13
RP7-7	R		S.A/D.18.+	4
RP1-7	CV		INTERLVD.+	11



REFERENCE DESIGNATION	DEVICE TYPE	GND PIN	+5V PIN	UNUSED OUTPUT PINS
B3, D5, F4, K3, K11	74 S 00	7	14	B3, D5, F4, K3, K11, K11-B
B2, H4	74 S 02	7	14	B2, H4, I3
J3	74 LS 02	7	14	J3-4, I0
C4, H5	74 S 04	7	14	
H3	74 LS 04	7	14	H3-B
D4, F5	74 LS 21	7	14	D4, F5-B
J9	74 LS 27	7	14	
J8	74 S 30	7	14	
D3, J4	74 S 32	7	14	D3, J4
J10	74 S 37	7	14	
H10	74 S 74	7	14	
A2	74 LS 74	7	14	
E4, F3, H9	74 S 109	8	16	
G4, G5, G6, G7	74 LS 109	8	16	
K4	74 S 112	8	16	K4-5,6
B1	74 LS 125	7	14	
G8	74 LS 133	8	16	
F6, H6	74 S 138	8	16	
E3	74 S 139	8	16	
H11	74 S 140	7	14	
K5	74 S 151	8	16	
C5	74 S 153	8	16	
G3, J5, J6, J7	74 LS 161	8	16	
E5	74 S 240	10	20	
G9, K12	74 LS 240	10	20	
A10, A11, B1, C1, D1, E11, H12, J12	74 S 241	10	20	A11-3, 5, 7, 9
A3, A4, A7, B4, B12, C12, E12, F7, G10, J11	74 LS 244	10	20	
C6, C9, D9, E7	74 S 280	10	20	
A5, B7, D7, D8, E6, F9	74 LS 280	10	20	
D2, F10, H2, K7	74 S 374	10	20	
A6, A8, A9, A12, B10, C10, D10, D12, E10, F2, F8, F11, F12, G11, G12, H7, K2, K10	74 LS 374	10	20	
C1, C2, D1, E1, F1, G1, H1, J1, J2, K6	27 S 21	8	16	
B5, B6, D6, K8, K9	63 S 241	8	16	
B8, B9, C7, C8, E8, E9	93 S 16	8	16	
RP1-9				1

NOTES: UNLESS OTHERWISE SPECIFIED
 1. CAPACITORS ARE .01 μF, 50 V.
 2. RESISTORS ARE IN OHMS 1/4 W, ± 5%
 3. RESISTORS IN RP3, RP6, RP7, RP8 ARE 1 K 1/2 W PER PACK, ± 2%
 4. RESISTORS IN RP1, RP2, RP4, RP5 ARE IN OHMS, 2 W PER PACK ± 5%.

REFERENCE DESIGNATION	NEXT ASSY	USED ON
E41		
RP-9		
R1		
C66		
LAST USED	NOT USED	

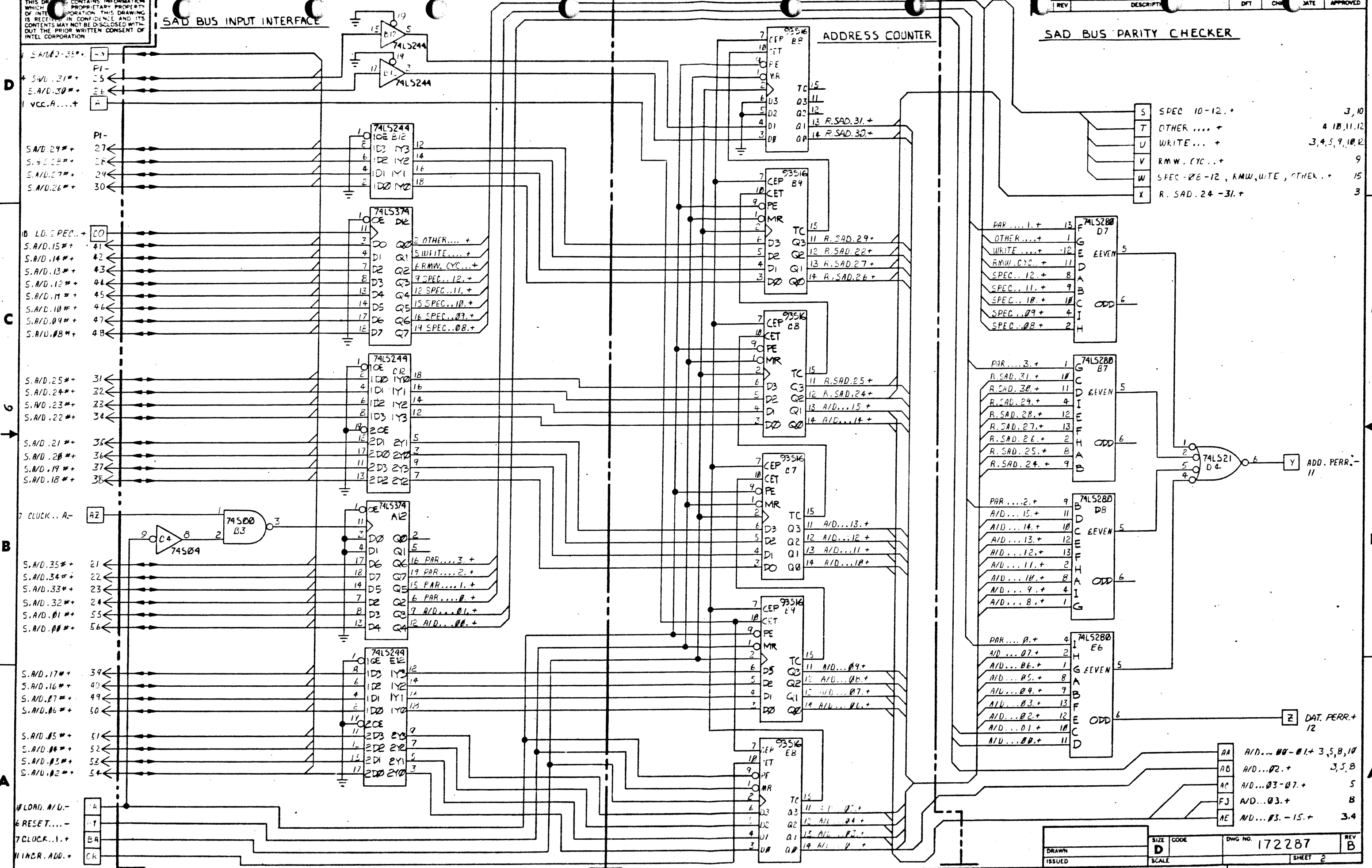
ITEM NO.	PART NUMBER	DESCRIPTION
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. BREAK ALL SHARP EDGES. DO NOT SCALE DRAWING. TOLERANCES: ANGLES ± 2° XX ± .00 XXX ± .010 SURFACE FINISH J		
SIGNATURE	DATE	3055 BOWERS AVE. SANTA CLARA, CALIF. 95051 LOGIC DIAGRAM, PWA, iSBC 432/604, MC
DRN BY TEL PALMER	11 24 61	
CHK BY		
ENGR APVD		
APVD		SIZE CODE D 01DD
QUANTITY PER DASH NO.		DWT NO. 172287
PARTS LIST		REV B
SCALE NONE		SHEET 1 OF 15

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SAD BUS INPUT INTERFACE

REV	DESCRIPTION	DFT	CHK	DATE	APPROVED

SAD BUS PARITY CHECKER



S	SPEC 10-12. +	3, 10
T	OTHER +	4, 10, 11, 12
U	WRITE ... +	3, 4, 5, 9, 10, 12
V	RMW. CYC... +	9
W	SPEC-08-12, RMW, WTE, OTHER... +	15
X	R. SAD. 24-31. +	3

PAR ... 1. +	13	F	74LS280 D7
OTHER ... +	1	G	EVEN 5
WRITE ... +	12	E	
RMW. CYC... +	11	D	
SPEC... 12. +	8	A	
SPEC... 11. +	9	B	
SPEC... 10. +	10	C	ODD 6
SPEC... 09. +	4	J	
SPEC... 08. +	2	H	

PAR ... 3. +	1	G	74LS280 B7
R. SAD. 31. +	10	C	EVEN 5
R. SAD. 30. +	11	D	
R. SAD. 29. +	4	I	
R. SAD. 28. +	12	E	
R. SAD. 27. +	13	F	
R. SAD. 26. +	2	H	ODD 6
R. SAD. 25. +	8	A	
R. SAD. 24. +	9	B	

PAR ... 2. +	9	B	74LS280 DB
A/D ... 15. +	11	D	EVEN 5
A/D ... 14. +	10	C	
A/D ... 13. +	12	E	
A/D ... 12. +	13	F	
A/D ... 11. +	2	H	ODD 6
A/D ... 10. +	8	A	
A/D ... 9. +	4	I	
A/D ... 8. +	1	G	

PAR ... 0. +	4	I	74LS280 E6
A/D ... 07. +	2	H	EVEN 5
A/D ... 06. +	1	G	
A/D ... 05. +	8	A	
A/D ... 04. +	9	B	
A/D ... 03. +	13	F	
A/D ... 02. +	12	E	ODD 6
A/D ... 01. +	10	C	
A/D ... 00. +	11	D	

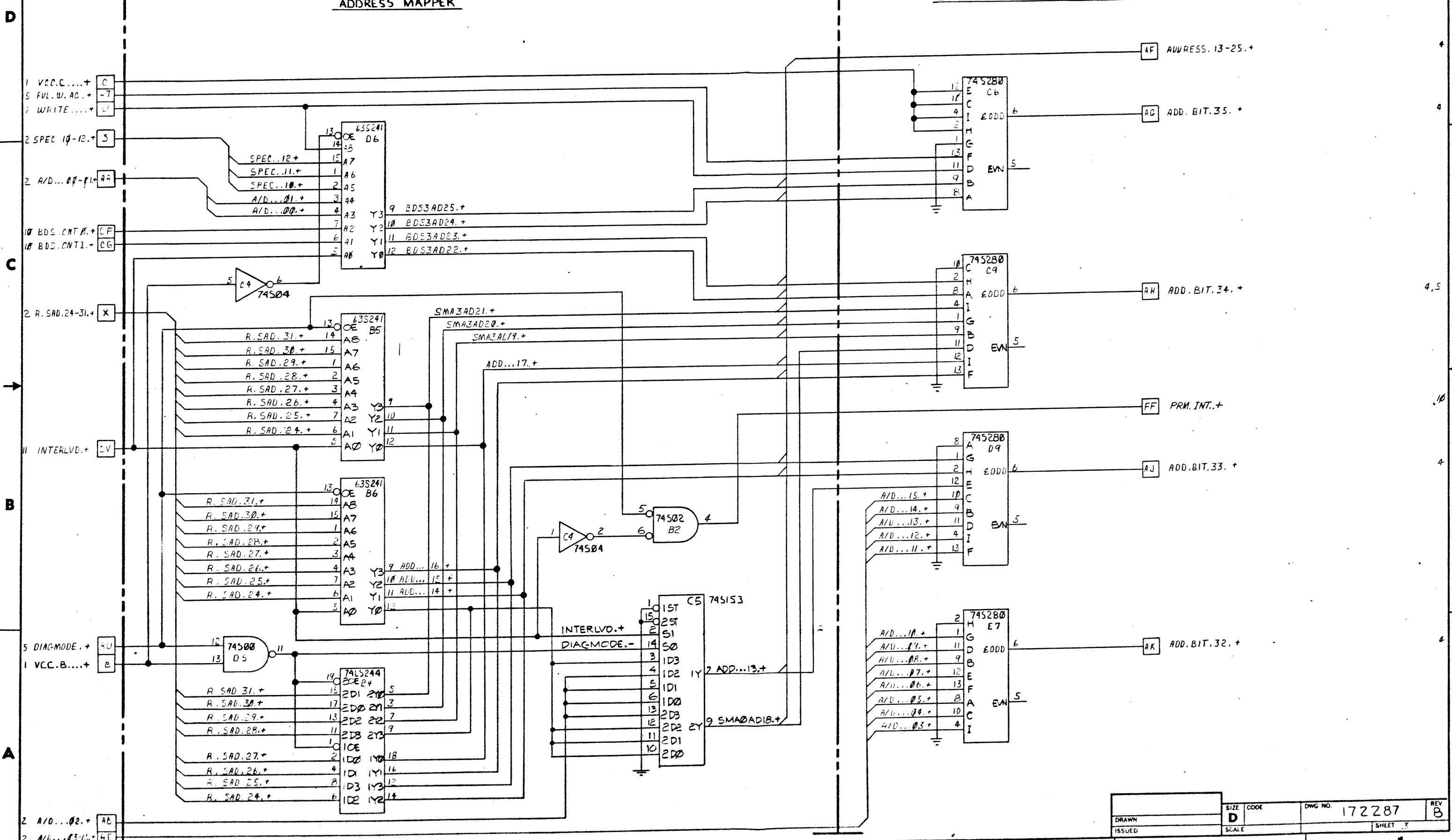
AA	A/D ... 00-01. +	3, 5, 8, 10
AB	A/D ... 02. +	3, 5, 8
AC	A/D ... 03-07. +	5
FJ	A/D ... 03. +	8
AE	A/D ... 03-15. +	3, 4

DRAWN	ISSUED	SIZE	CODE	DWG NO.	REV
		D		172287	B
		SCALE		SHEET	2

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ADDRESS MAPPER

SA ADDRESS PARITY GENERATORS



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ADDRESS MAPPER (CONT.)

SAD BUS OUTPUT INTERFACE

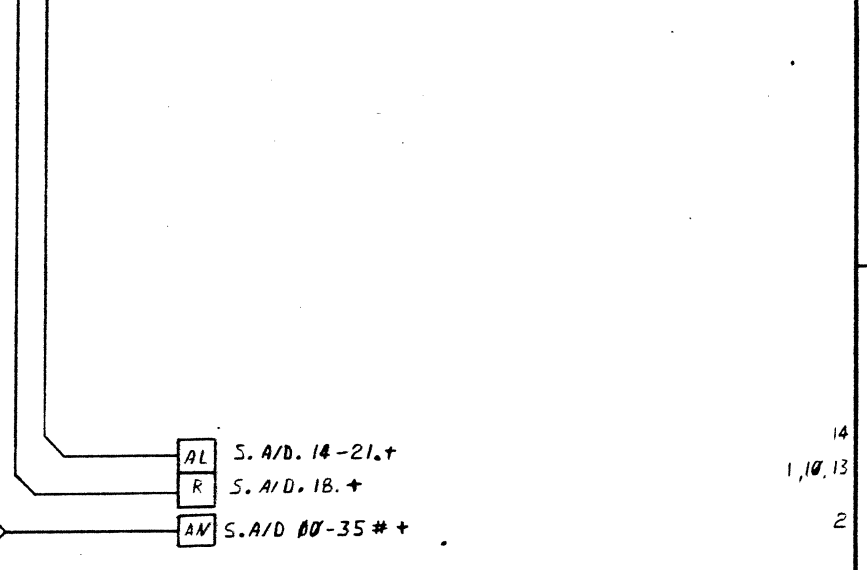
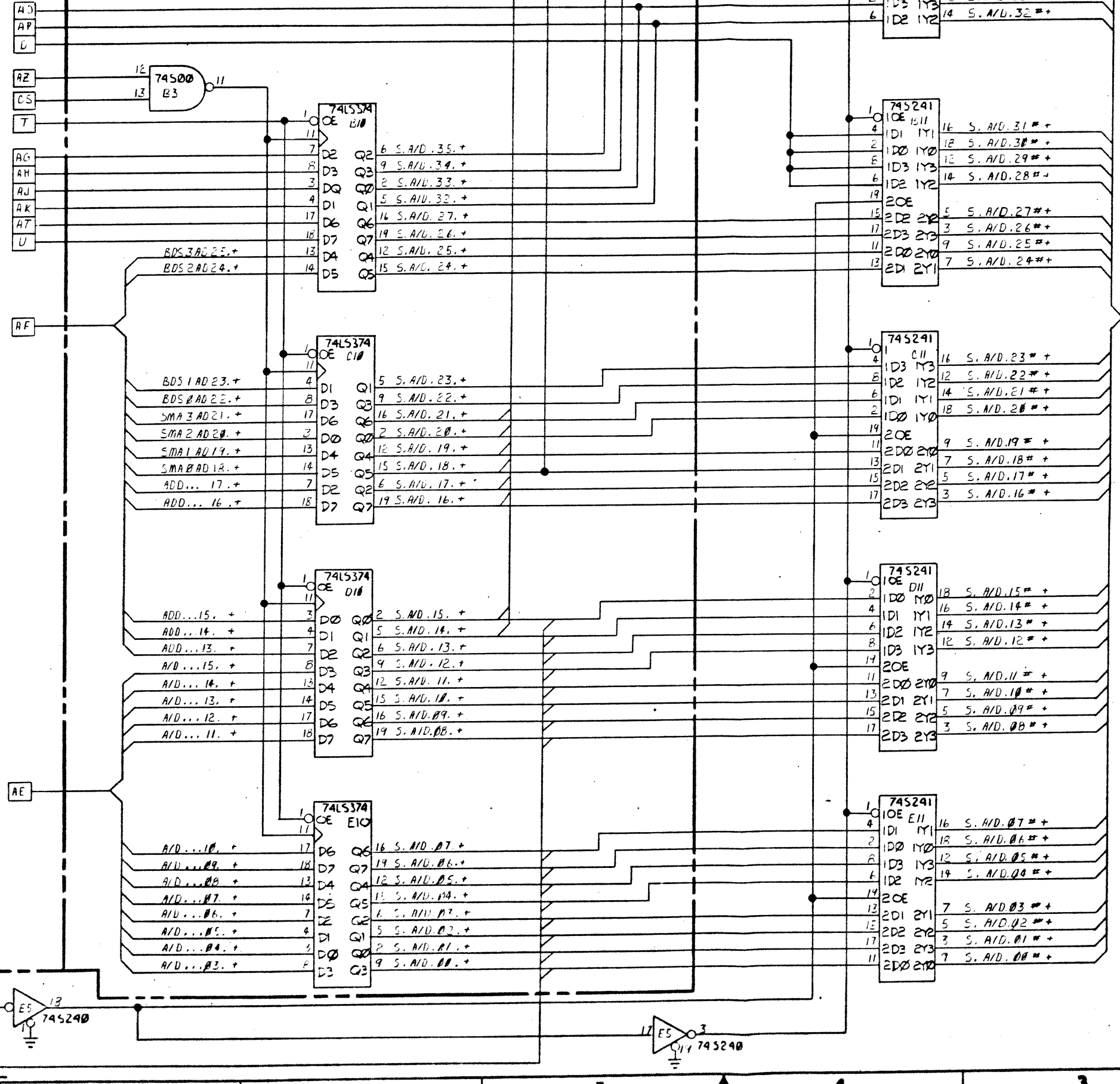
- 5 S.A/D.33 +
- 5 S.A/D.32 +
- 1 VCC.D....+
- 7 CLDCK.A-
- 11 LD. OUTRG.+
- 2 OTHER....+
- 3 ADDBIT 35.+
- 3 ADDBIT 34.+
- 3 ADDBIT 33.+
- 3 ADDBIT 32.+
- 5 FUL.W.AC.+
- 2 WRITE....+

- AD
- AP
- U
- AZ
- CS
- T
- AG
- AH
- AJ
- AK
- AT
- U

- AF
- AE

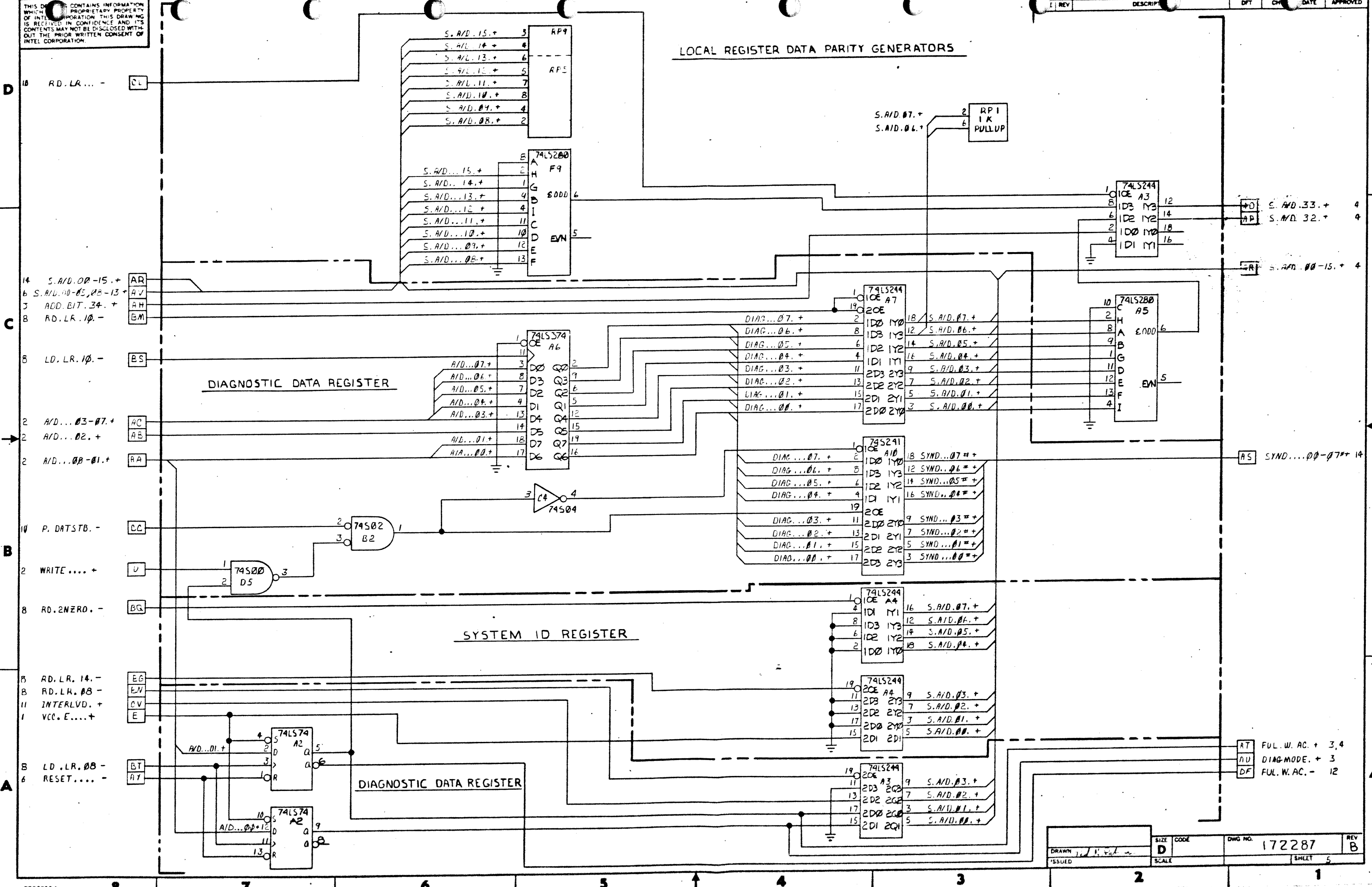
- BDS 3 AD 25.+
- BDS 2 AD 24.+
- BDS 1 AD 23.+
- BDS 0 AD 22.+
- SMA 3 AD 21.+
- SMA 2 AD 20.+
- SMA 1 AD 19.+
- SMA 0 AD 18.+
- ADD... 17.+
- ADD... 16.+
- ADD... 15.+
- ADD... 14.+
- ADD... 13.+
- A/D... 15.+
- A/D... 14.+
- A/D... 13.+
- A/D... 12.+
- A/D... 11.+
- A/D... 10.+
- A/D... 09.+
- A/D... 08.+
- A/D... 07.+
- A/D... 06.+
- A/D... 05.+
- A/D... 04.+
- A/D... 03.+

- FE
- FE



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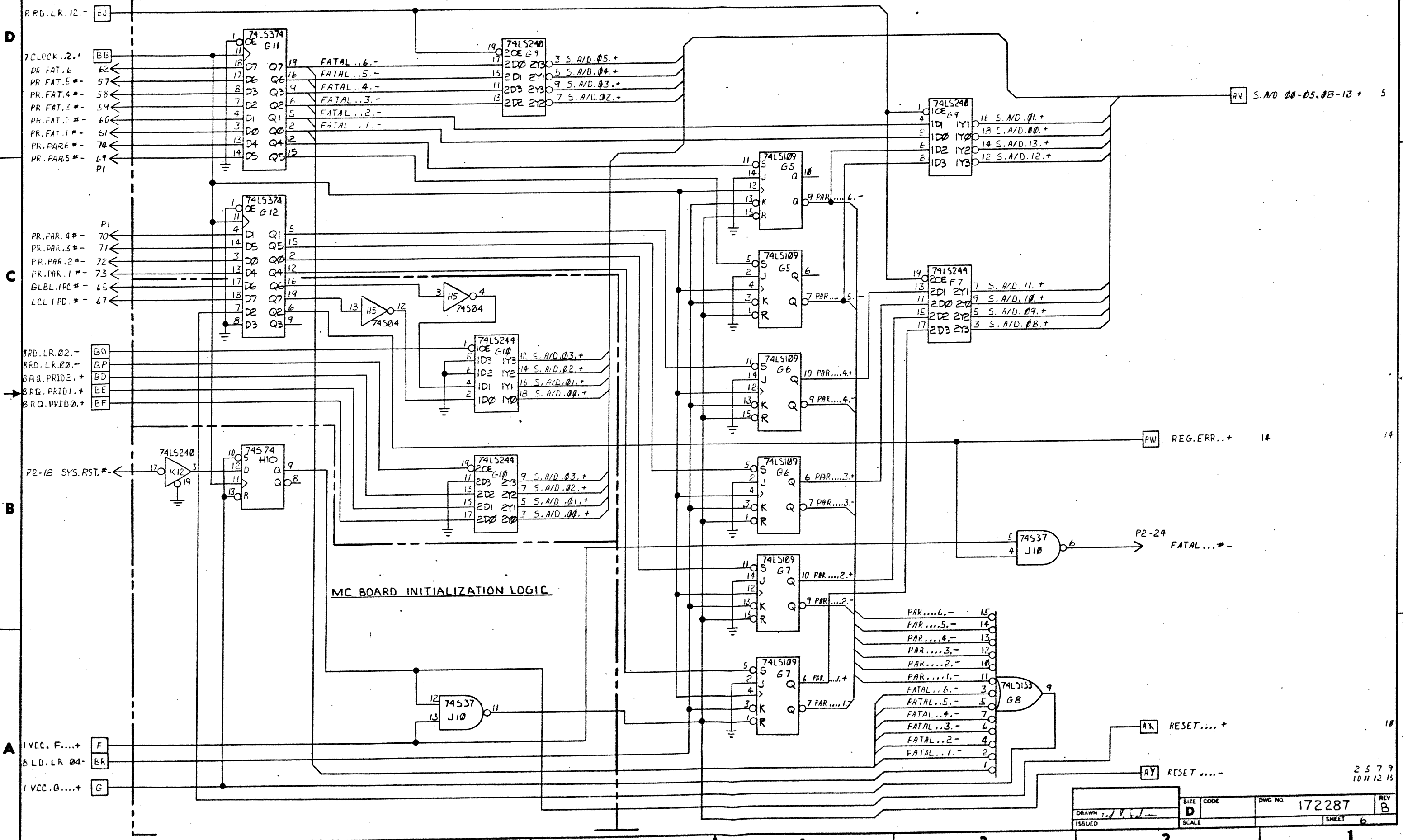
LOCAL REGISTER DATA PARITY GENERATORS



REV	5	B
SIZE	D	CODE
SCALE		
DWG NO.	172287	
REV	B	
ISSUED		SHEET 5

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PROCESSOR ERROR REGISTER



MC BOARD INITIALIZATION LOGIC

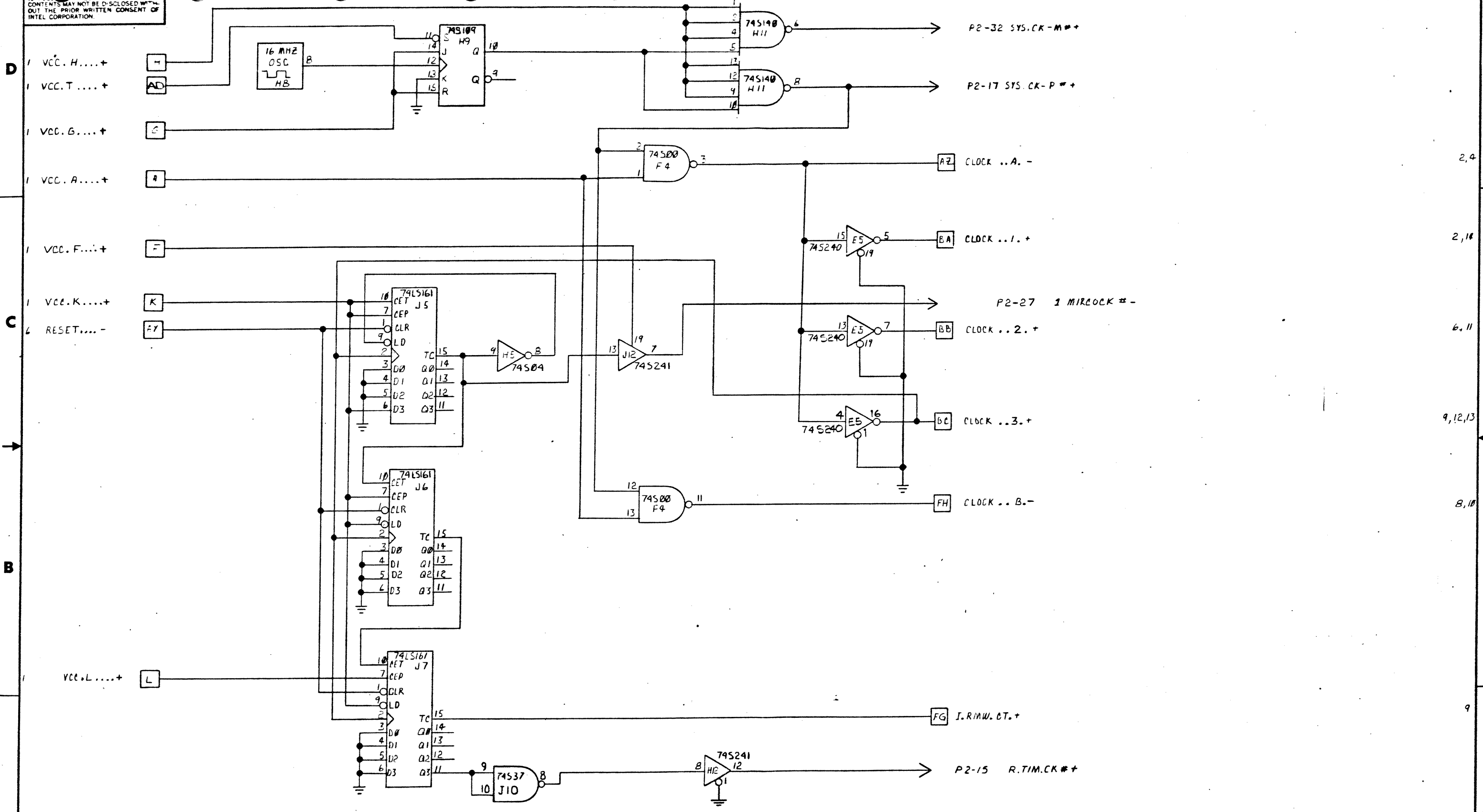
DRAWN	SIZE	CODE	DWG NO.	REV
ISSUED	D		172287	B
	SCALE		SHEET	6

2579
10 11 12 15

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CLOCK GENERATION LOGIC

REV	DESCRIP	REVISIONS	DFT	CH	DATE	APPROVED
E						

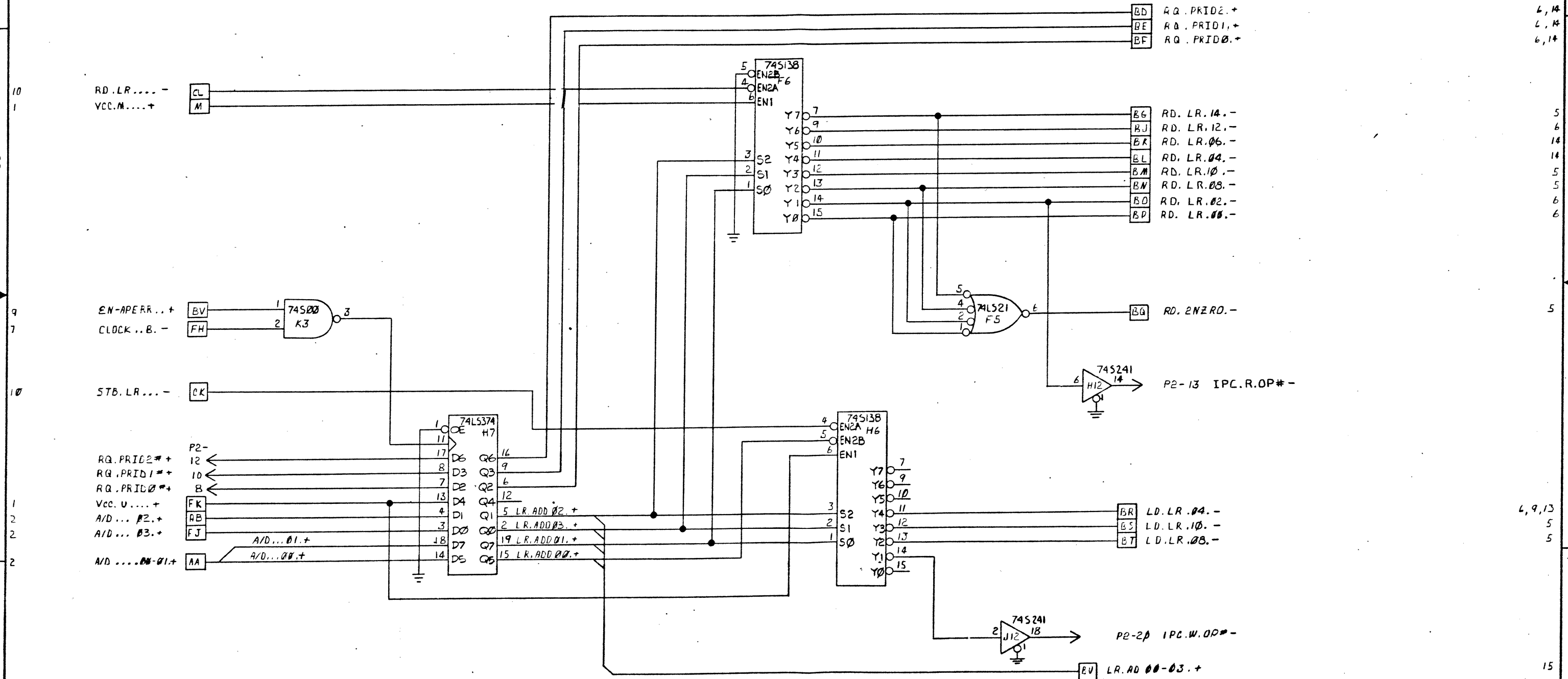


DRAWN	ISSUED	SIZE	CODE	DWG NO.	REV
		D		172287	B
				SHEET	7

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LOCAL REGISTER DECODER

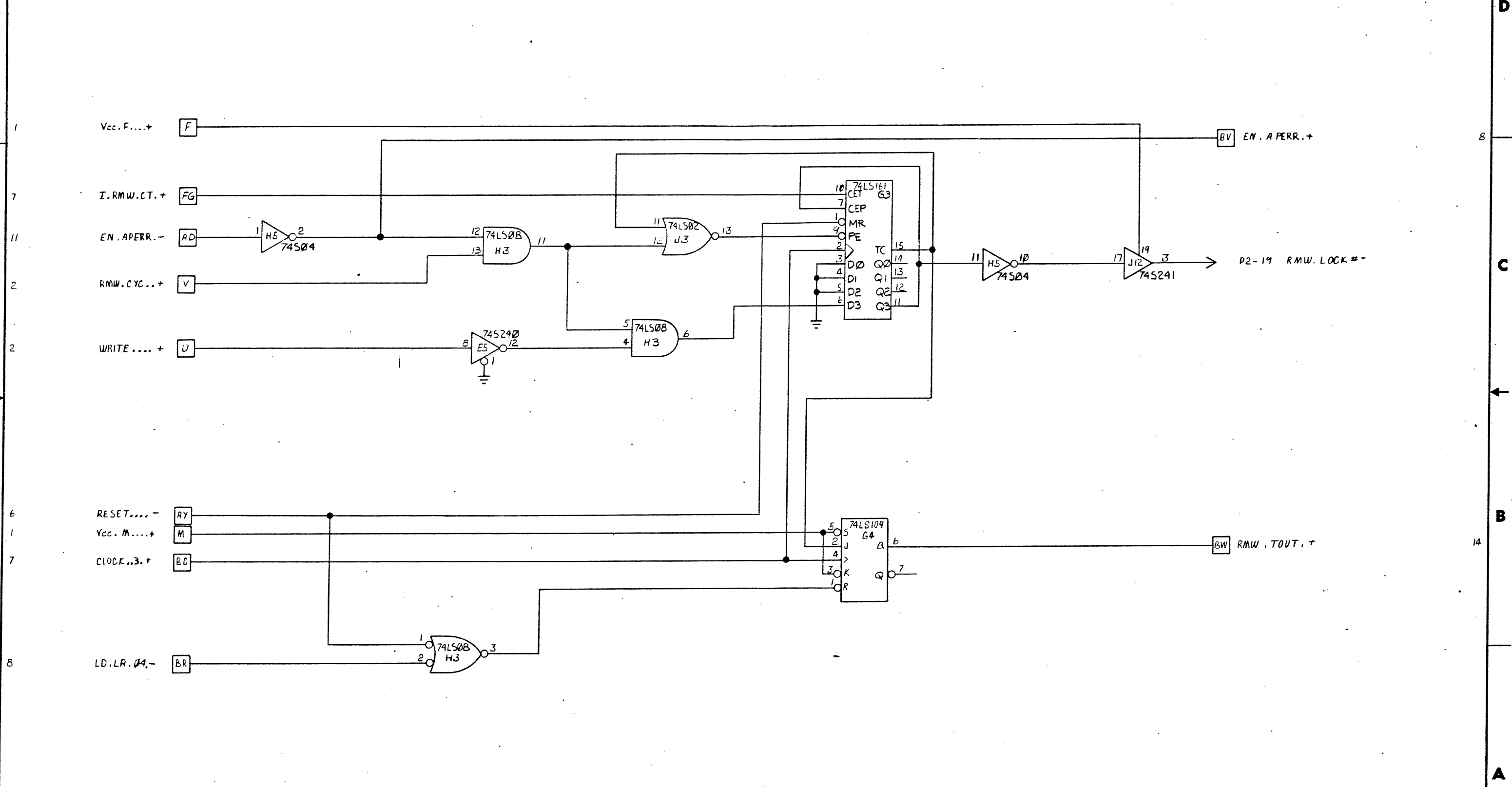
REV	DESCRIP	DFT	DATE	APPROVED
1				



DRAWN	CODE	DWG NO.	REV
ISSUED	SCALE	172287	B

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RMW LOCK AND TIMEOUT LOGIC

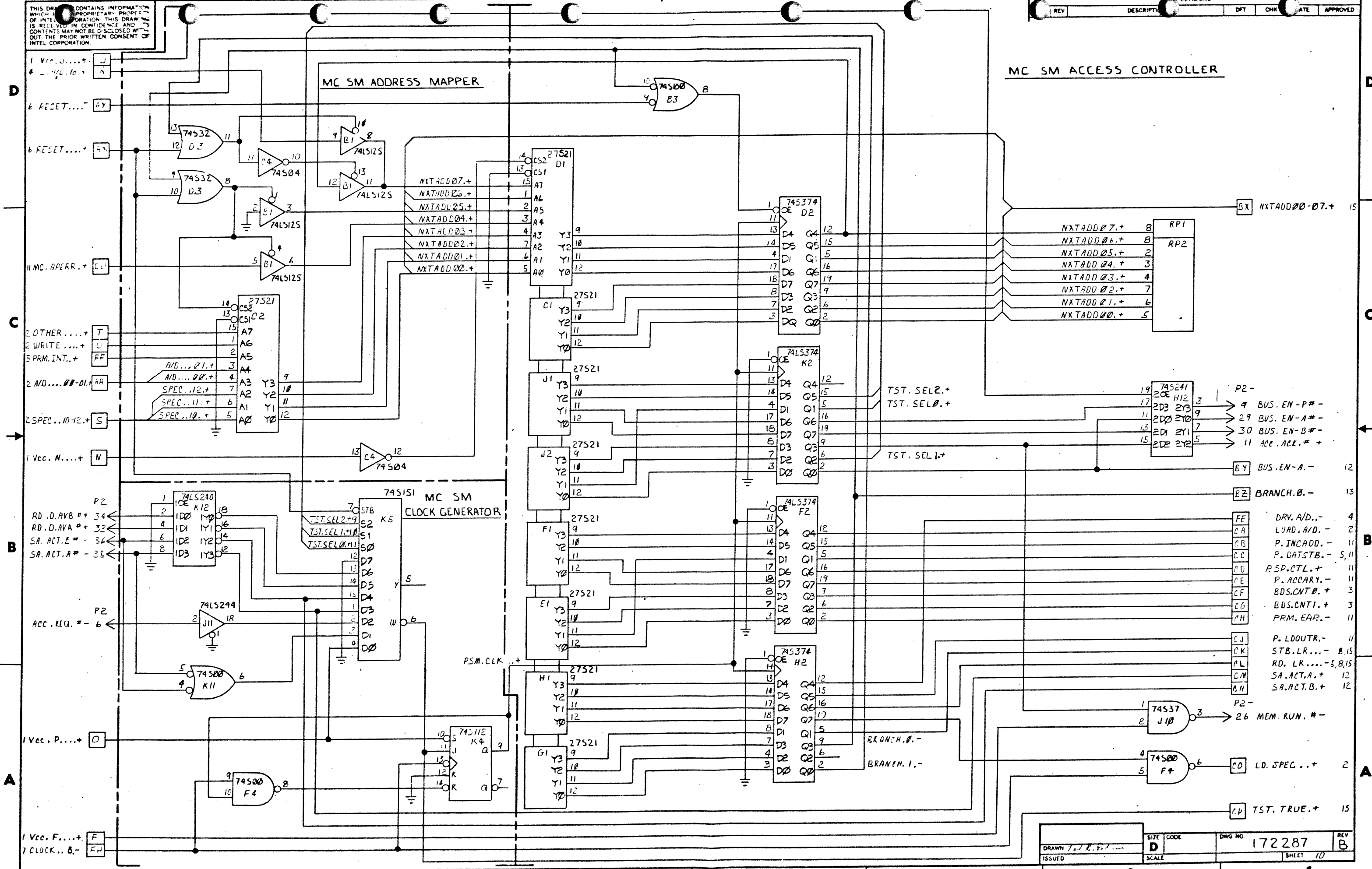


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MC SM ACCESS CONTROLLER

MC SM ADDRESS MAPPER

MC SM CLOCK GENERATOR

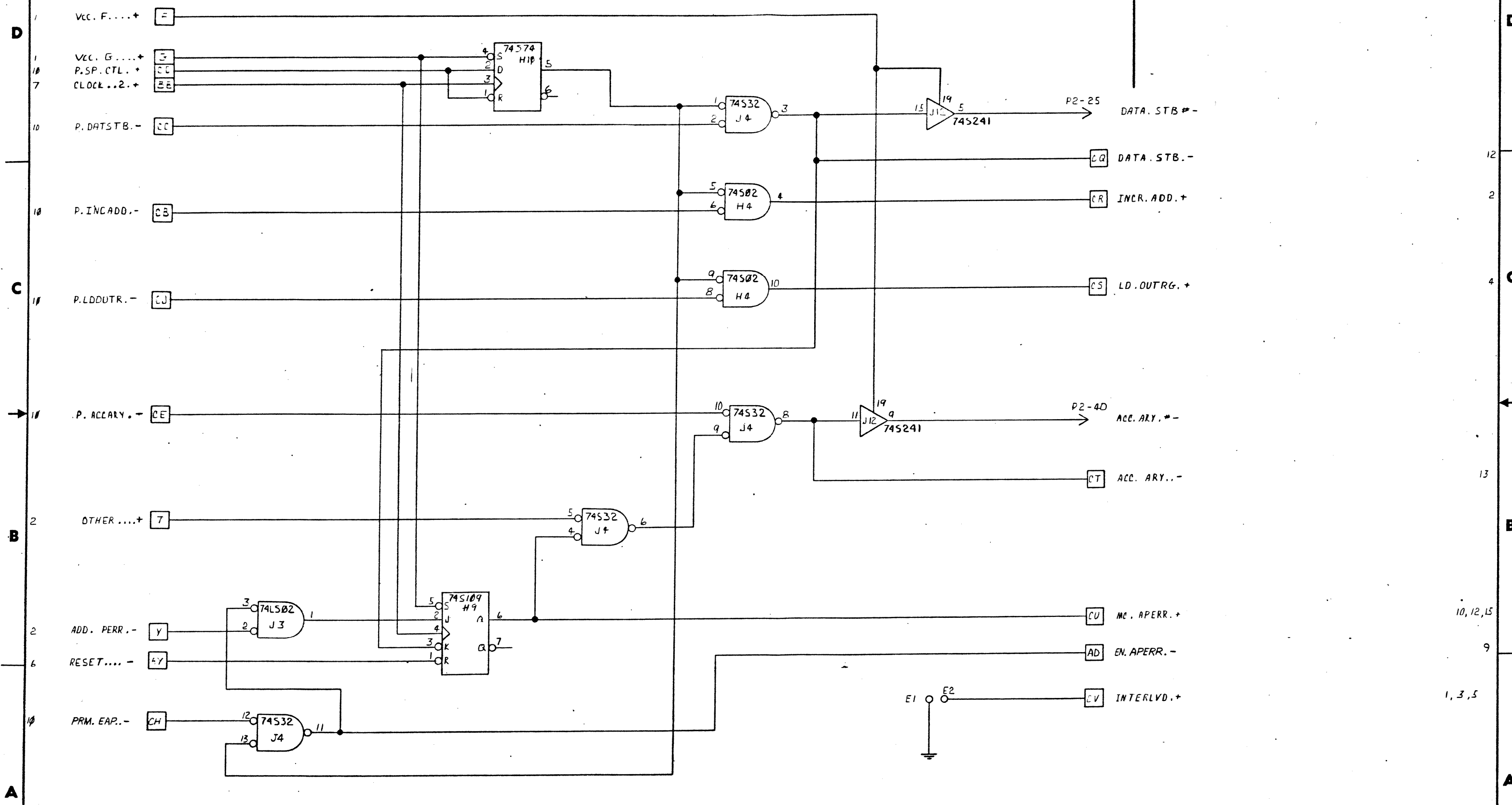


DRAWN	SIZE	CODE	DWG NO.	REV
ISSUED	D		172287	B
	SCALE		SHEET 10	

MC SM ACCESS CONTROLLER (CONT.)

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REV	DESCR	DFT	DATE	APPROVED
11	B			

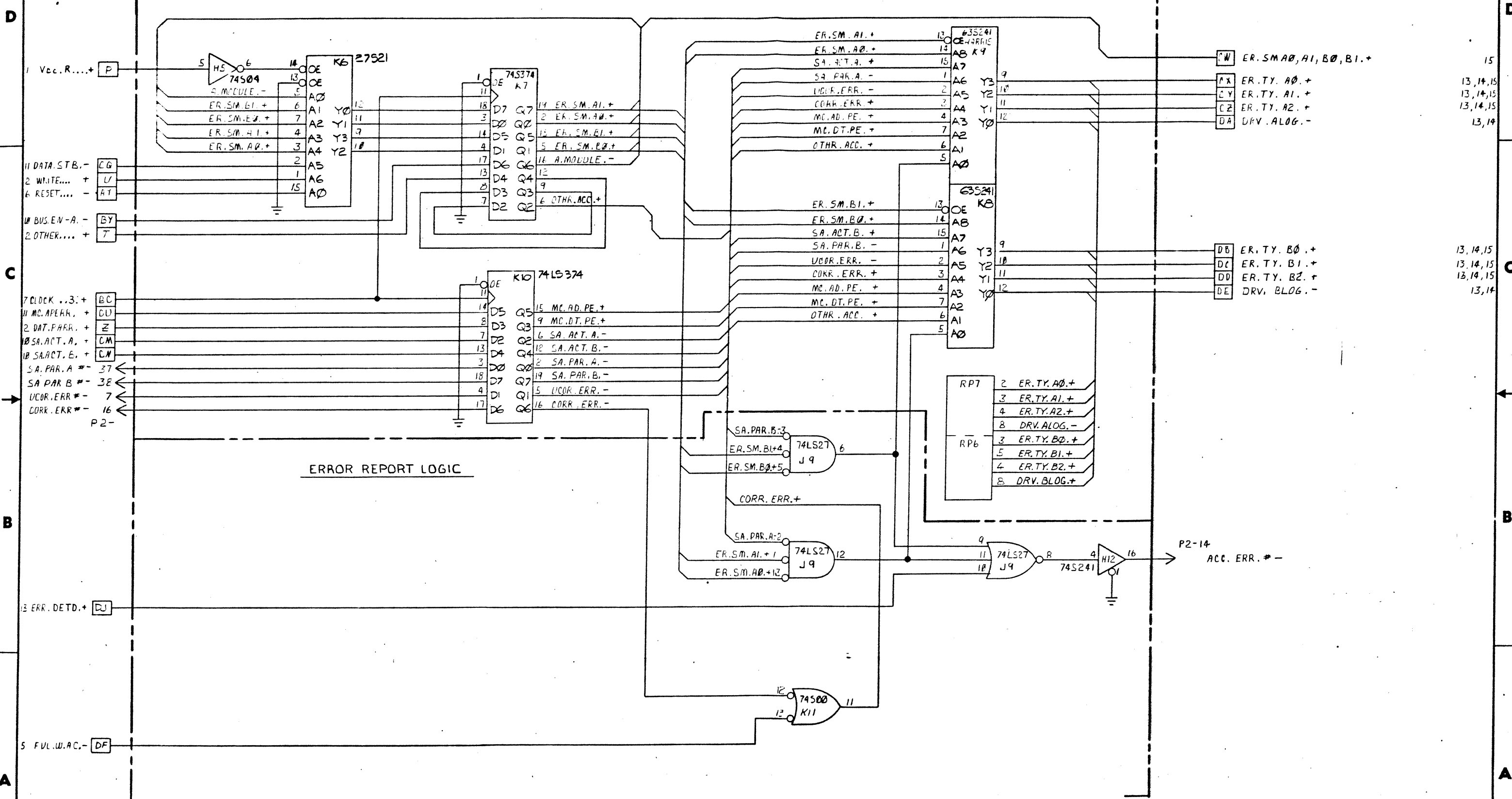


DRAWN <i>F. J. Kelly</i>	SIZE D	CODE	DWG NO. 172287	REV B
ISSUED	SCALE		SHEET 11	

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ERROR LOG STATE MACHINES

REV	DESCRIPTION	DFT	CHK	DATE	APPROVED
1					



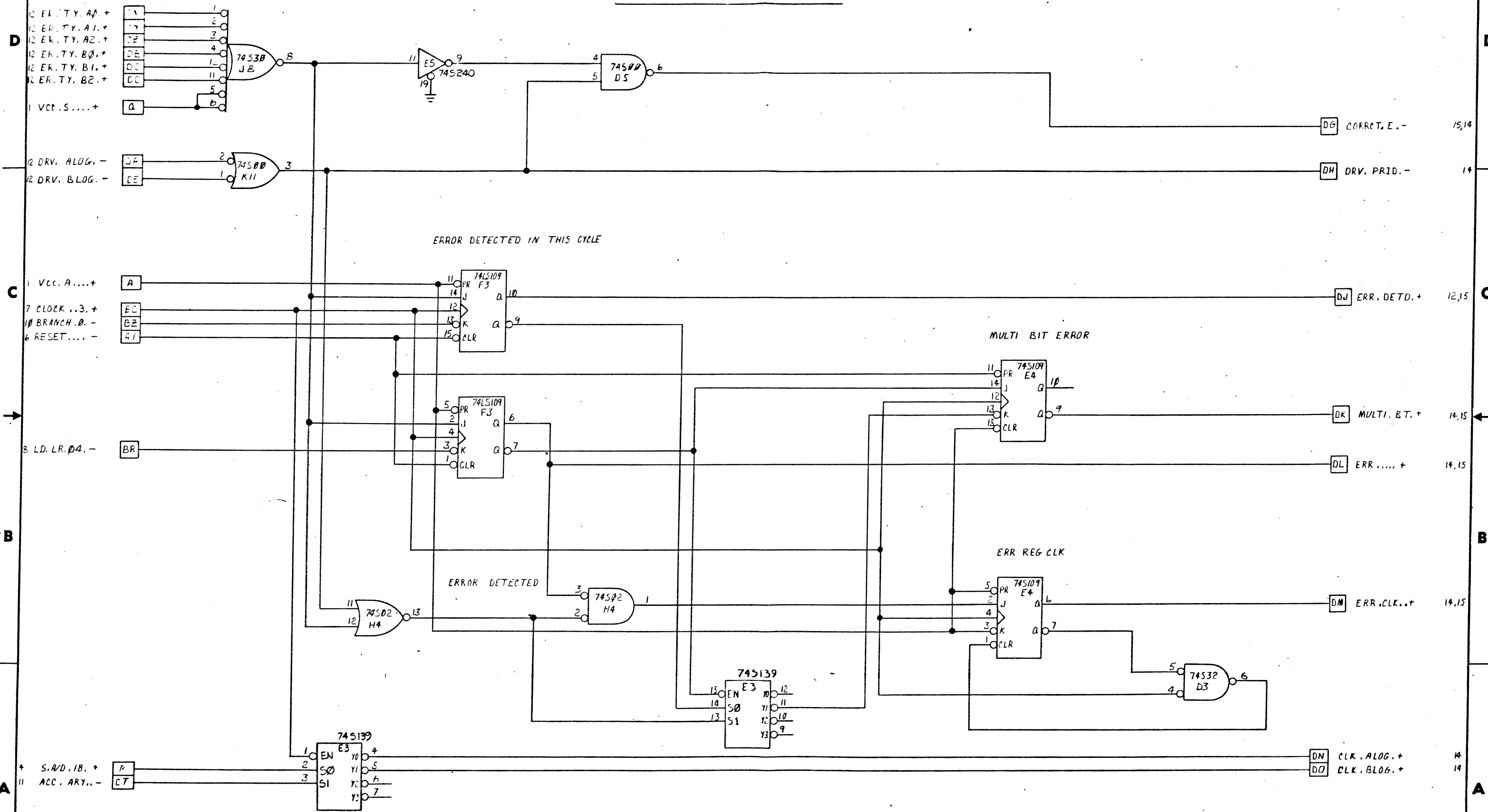
ERROR REPORT LOGIC

DRAWN	SIZE	CODE	DWG NO	REV
ISSUED	D		172287	B
	SCALE		SHEET	12

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REV	REV	DESCRIP	DFT	CHK	DATE	APPROVED
1						

ERROR REPORT LOGIC (CONT.)

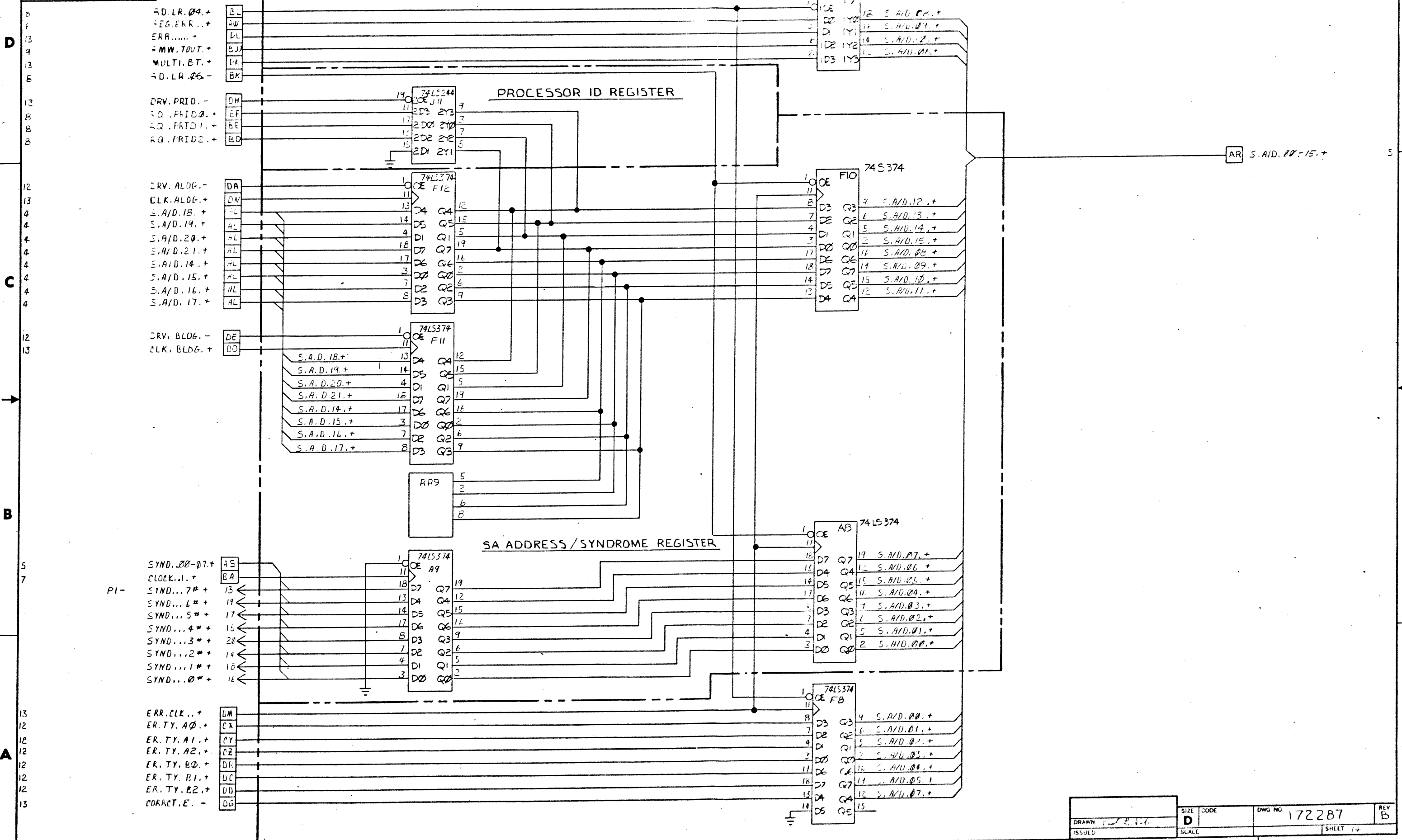


DRAWN	ISSUED	SIZE	CODE	DWG NO.	REV
		D		172287	B
		SCALE		SHEET 13	

SYSTEM ERROR REGISTER

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RELEASED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

REV	DESCR	DFT	DATE	APPROVED

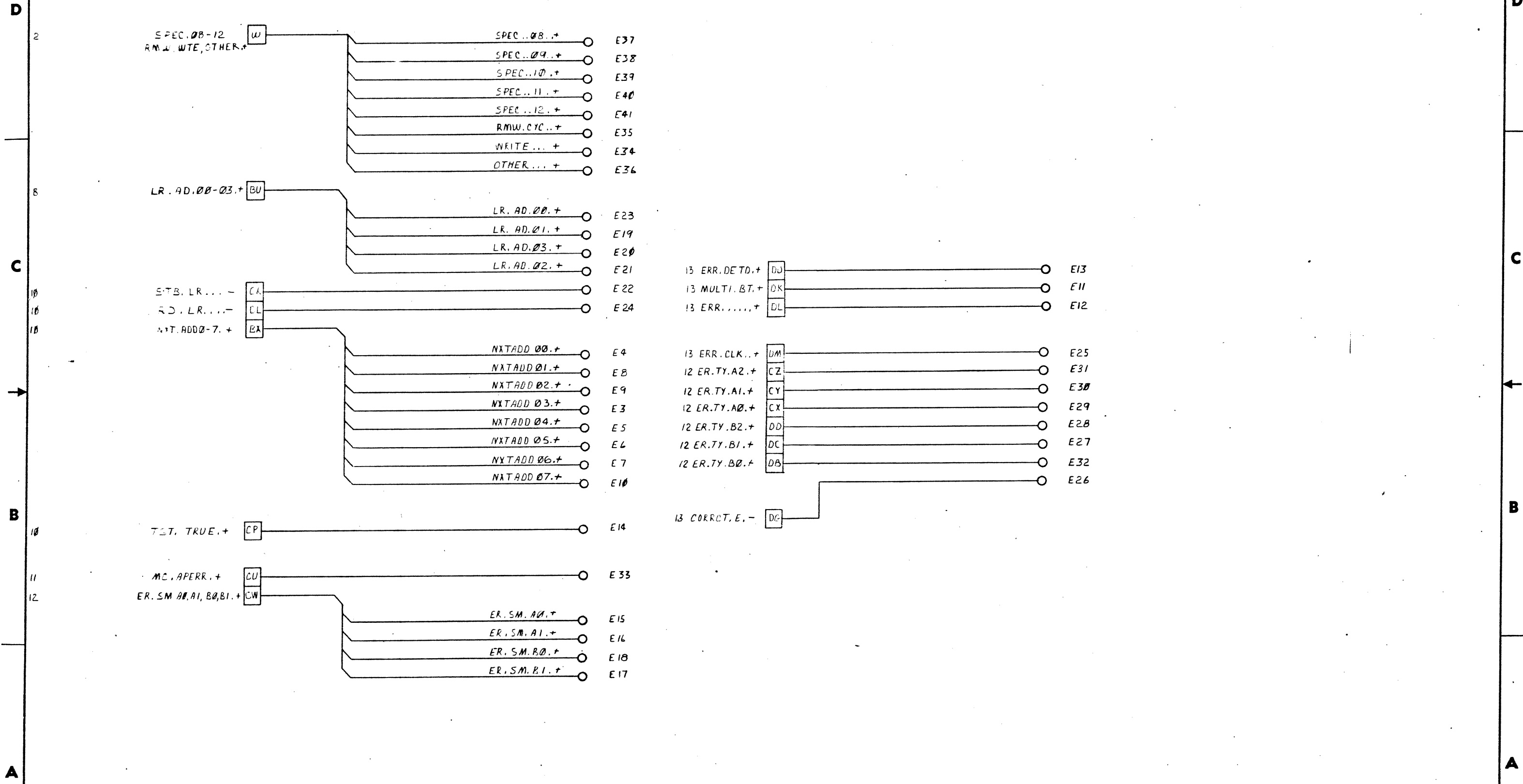


DRAWN	SIZE D	CODE	DWG NO 172287	REV B
ISSUED	SCALE		SHEET 14	

THIS DRAWING CONTAINS INFORMATION WHICH IS PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

REV	DESCRIP	DFT	DATE	APPROVED
E				

MC BOARD TEST POINTS

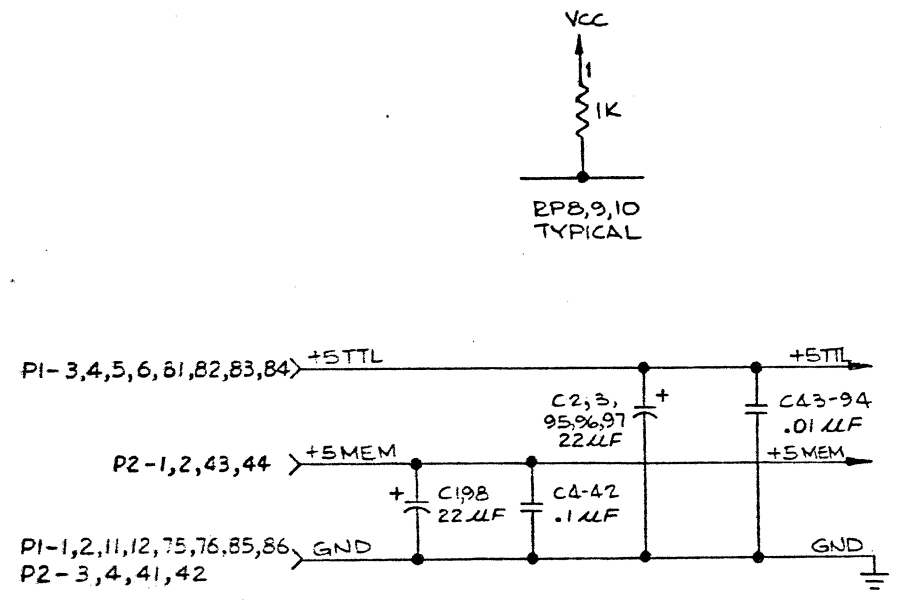


DRAWN	ISSUED	SIZE	CODE	DWG NO.	REV
		D		172287	B
				SHEET	15

THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPERTY OF INTEL CORPORATION. IT IS TO BE KEPT IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE WRITTEN CONSENT OF INTEL CORPORATION.

		REVISIONS				
NO.	DESCRIPTION	BY	DATE	CHK	APVD	DATE
A	PER DRF 12-12	DOCON	2/81	WLC	WLC	2/81
B	DRF 4-15	DS	5/81	WLC	WLC	5/81
C	PER ECO 12900	V.C.	9/81	WLC	WLC	9/81

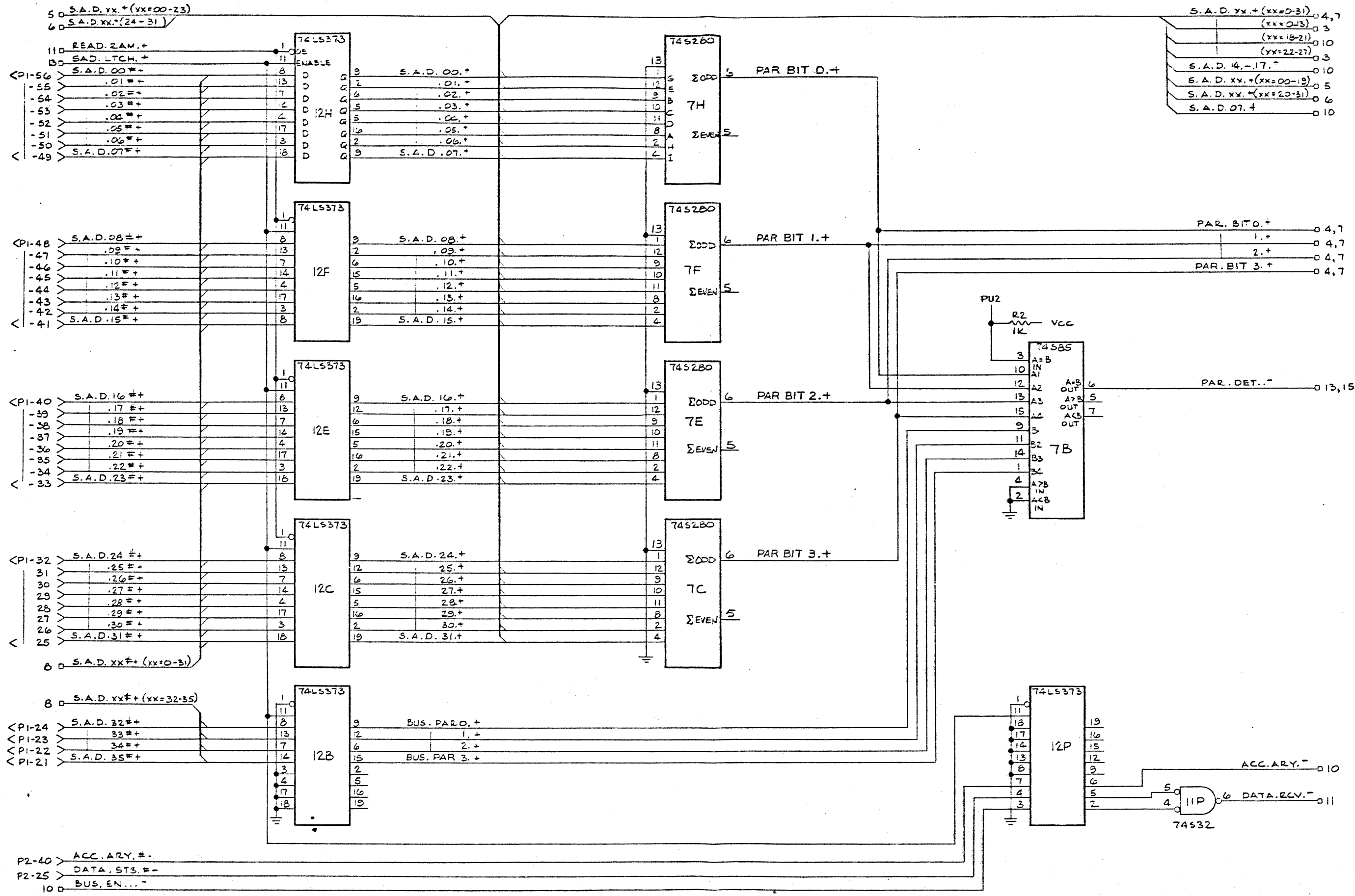
DEVICE LOCATOR					
TYPE	GND	-5V	REF DES	UNUSED OUTPUT PINS	
74S00	7	14	6K, 10J, 5P		
74S02	7	14	5K, 6P		
74S04	7	14	4A, 8K, 10P	4A-6, 8	
74S08	7	14	7D		
74S10	7	14	5A		
74S20	7	14	7J		
74S32	7	14	11P	11P-8, 3	
74S83	8	16	7B		
74S86	7	14	5C, 10C, 10E, 10F, 10H, 12K, 9B, 9C, 9E, 9F, 9H		
74S108	8	16	5P, 12, 2R, 9K		
74S112	8	16	2K, 9M		
74S138	8	16	8B, 8C, 8E, 8F, 8H		
74S151	8	16	4B, 5B, 6B, 8M		
74S158	8	16	6J, 9A, 10A		
74LS161	8	16	11K, 6M		
74S240	10	20	1L, 2L, 10B, 11B, 11C, 41E, 11E, 11H, 8A, 11A, 2N, 1P, 2B	10B-3, 5, 9, 12, 16, 18; 8A, 9; 11A-4, 6; 2P-4, 14; 11B-3, 5, 7, 14, 16, 18	
74S241	10	20	4E, 4F, 4H, 3A, 4C, 11M	3A-18; 11M-3, 7, 12, 14	
74S258	8	16	1M, 2M		
74S260	7	14	3A, 11J	11J-6	
74S280	7	14	6C, 6E, 6G, 6H, 7C, 6E, 6F, 6H, 7A		
74LS373	10	20	12A, B, C, E, F, H, P	12A-9; 12B-2, 5, 16, 19; 12P-9, 12, 15, 16, 19	
74LS374	10	20	12M	12M-9, 15, 16	
74S174	8	16	8J		
74LS377	10	20	5J	5J-6, 19	
74LS393	7	14	1N		
50ns DELAY	8	16	5M, 10M, 9P		
PROM			7M		
2118	16	8	2AA-2WW; 1BB-1WW		
2132	16	8			
2133	16	8			
2164	16	8			

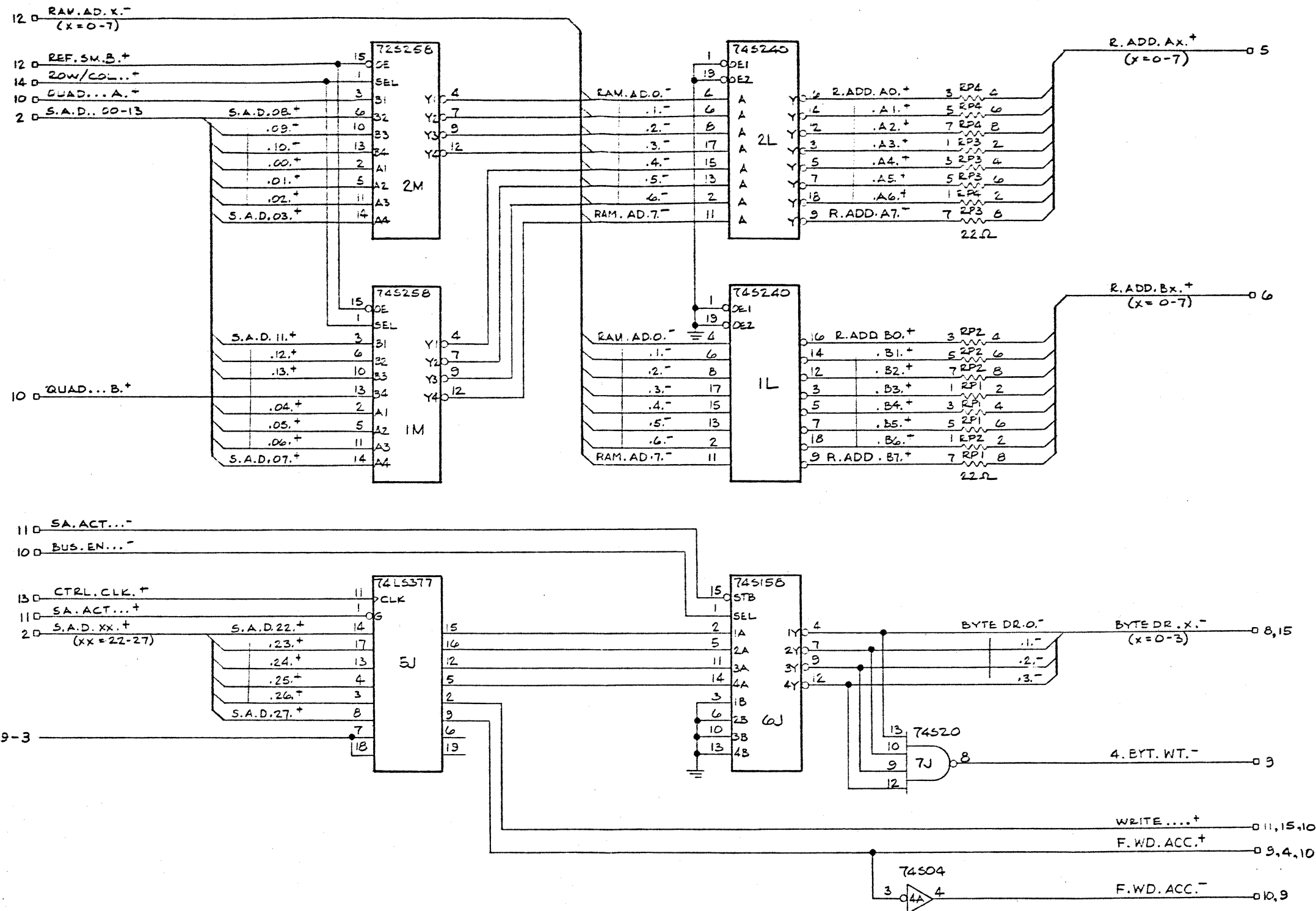


JUMPER TABLE		
DEVICE	CAPACITY	JUMPER
2118	64K BYTE	W2, W7, W12
2132	128K BYTE	
57231		W5, W7, W9
57232		W5, W7, W11
57233		W6, W7, W8
57234		W6, W7, W10
2164	256K BYTE	W5, W11

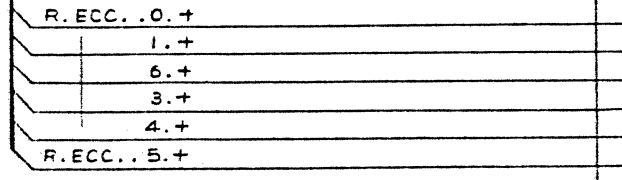
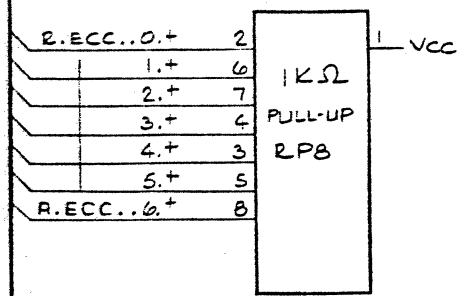
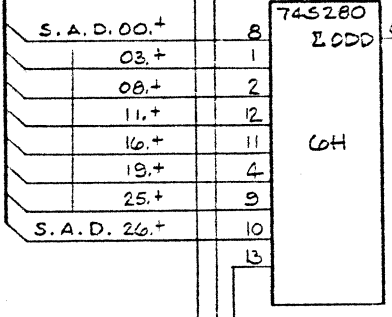
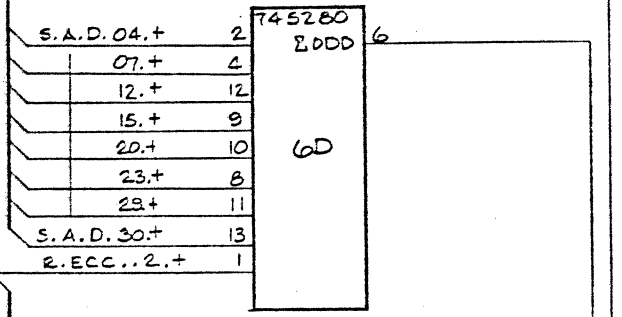
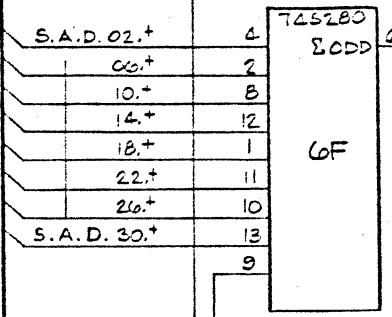
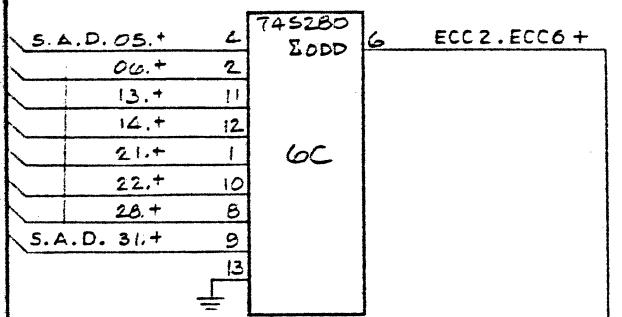
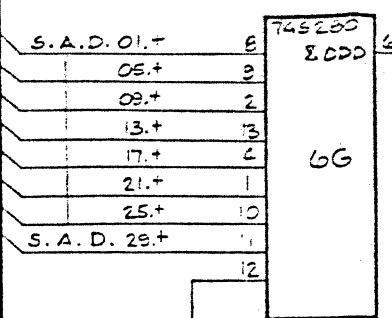
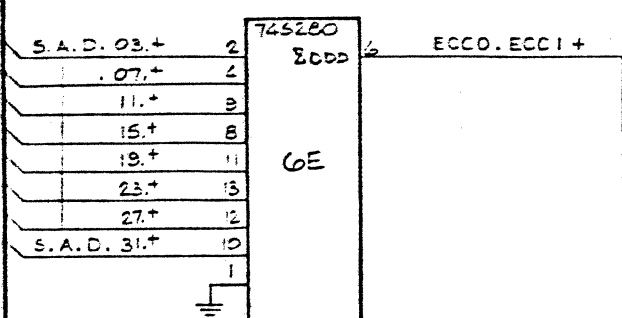
NOTES: UNLESS OTHERWISE SPECIFIED
 1. ALL RESISTANCE VALUES ARE IN OHMS 1/4W, 5%
 2. ALL CAPACITANCE VALUES IN MICROFARADS
 3. <PX-YY> SIGNIFIES BI-DIRECTIONAL SIGNALS

QUANTITY PER DASH NO		ITEM NO.	DESCRIPTION	
UNLESS OTHERWISE SPECIFIED:		PARTS LIST		
1. DIMENSIONS ARE IN INCHES.		SIGNATURE	DATE	 3065 BOWERS AVE SANTA CLARA CALIF. 95051
2. BREAK ALL SHARP EDGES.		DRN BY DOCON	2/81	
3. DO NOT SCALE DRAWING.		CHK BY [Signature]	5/81	
4. TOLERANCES:		ENGR APVD [Signature]	5/81	
ANGLES ±		APVD [Signature]	7/81	TITLE
XX ±				SCHMATIC DIAGRAM
XXX ±				LSBC432/205 STORAGE MODULE
				SIZE
				D 12 01 L
				SCALE NONE
				DOCUMENT NUMBER
				112338
				REV
				C
				SHEET 1 OF 15

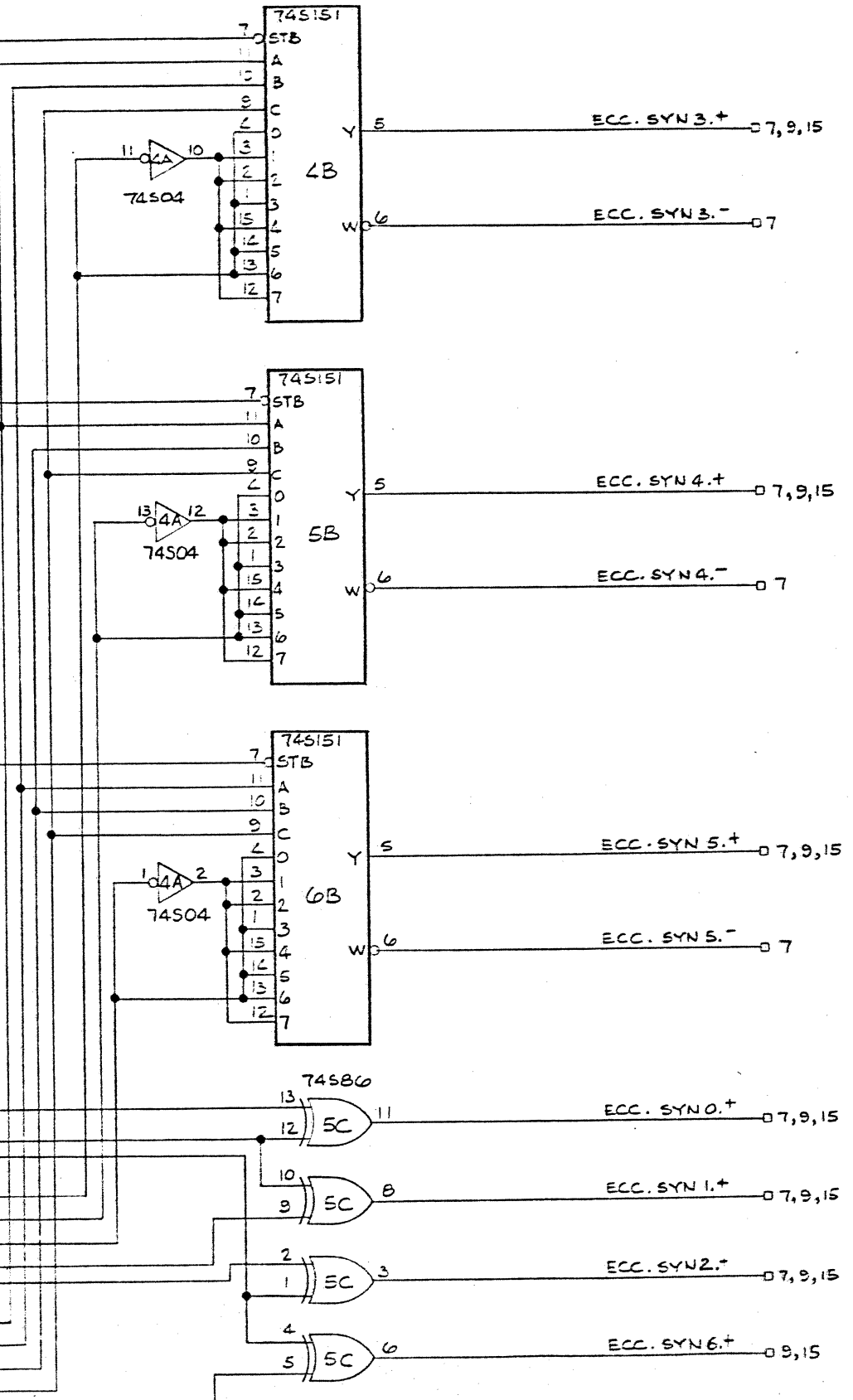




2 0 S.A.D. xx.+
(xx=0-31)



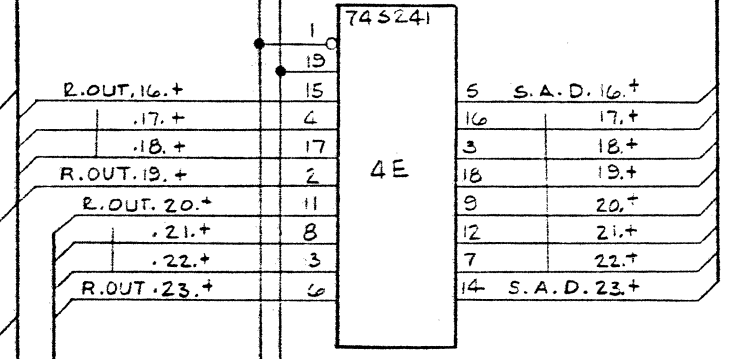
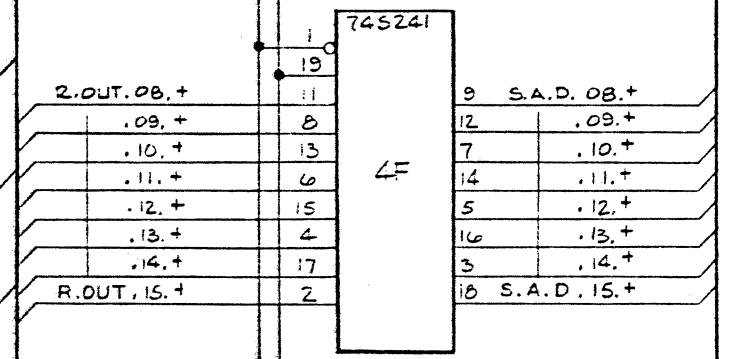
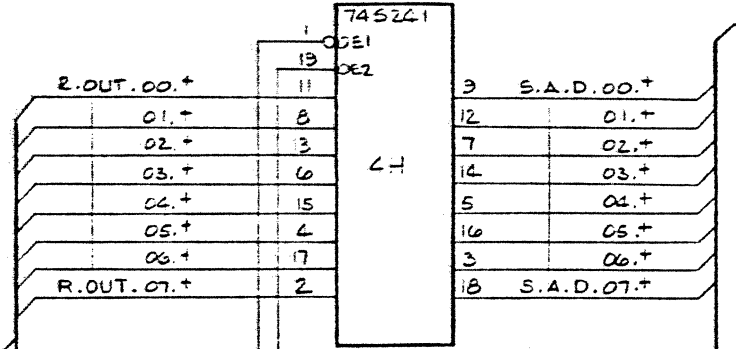
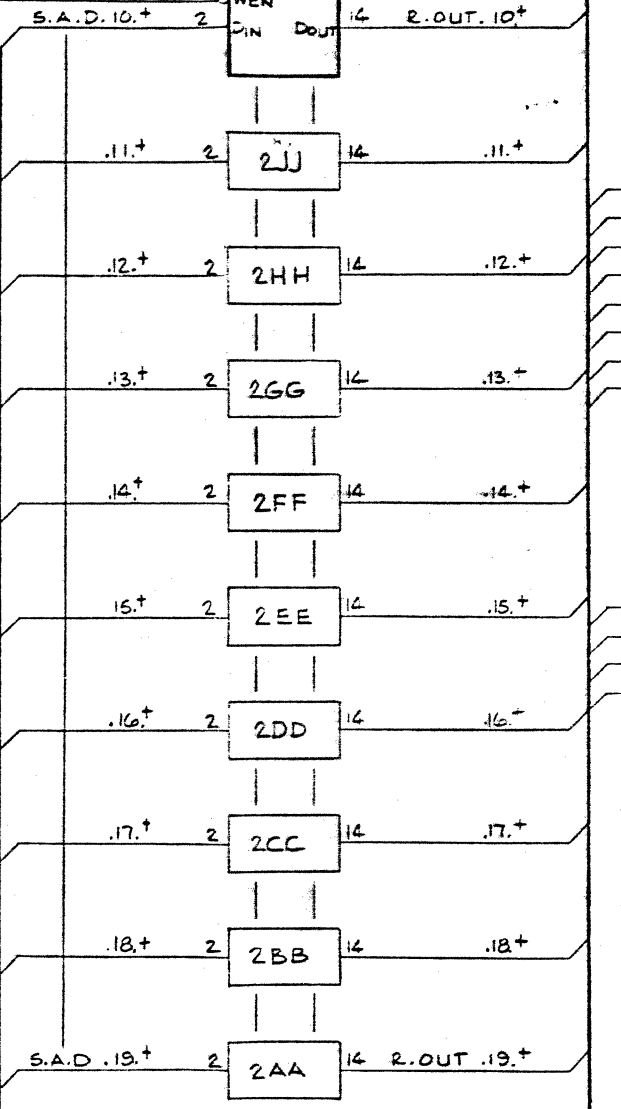
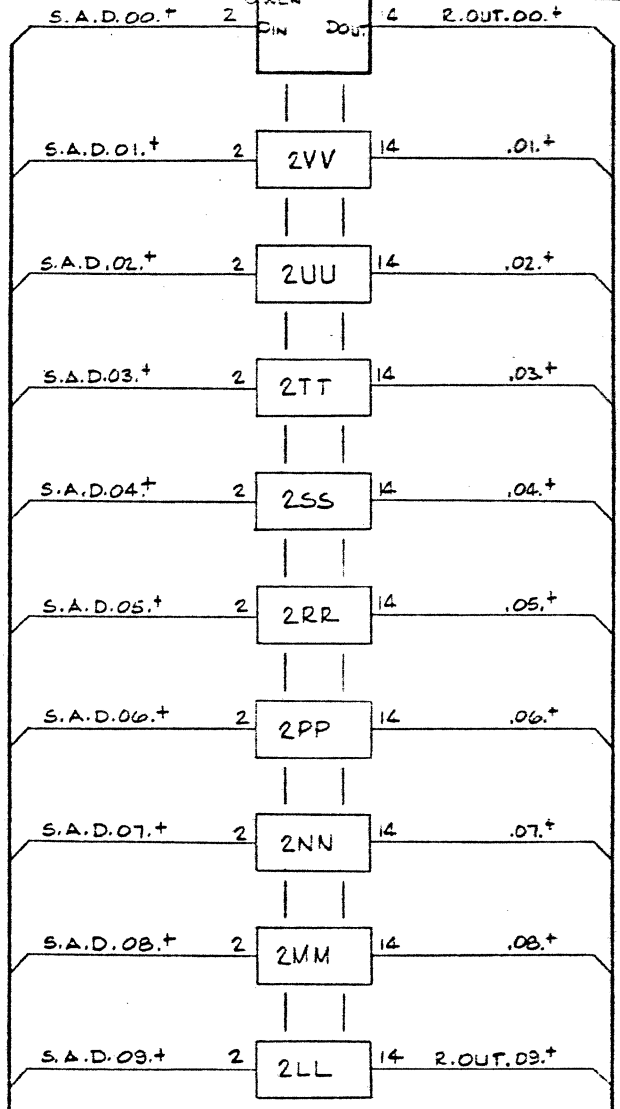
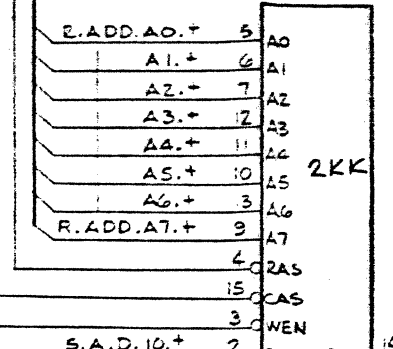
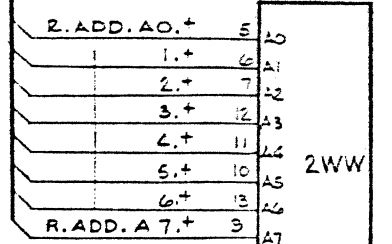
3 0 F.WD. ACC.+
2 0 PAR BIT 0.+
2 0 1.+
2 0 2.+
2 0 PAR BIT 3.+



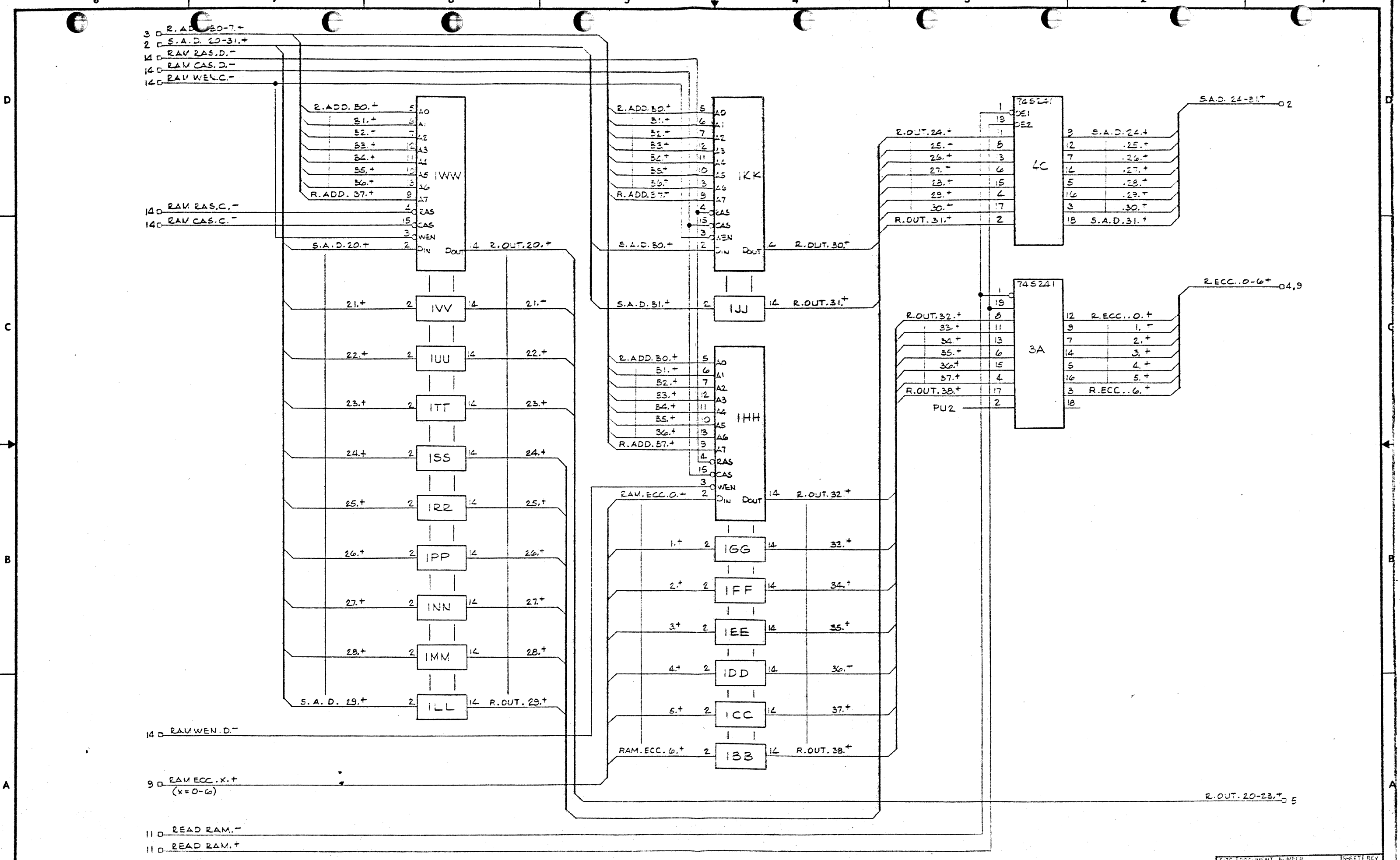
3 R.ADD.A0-7
 14 RAM.RAS.B.-
 14 RAM.CAS.B.-
 14 RAM.WEN.B.-

12 RAM.RAS.A.-
 14 RAM.CAS.A.-
 14 RAM.WEN.A.-

2 S.A.D.00-19
 6 R.OUT.20-23.+
 11 READ.RAM.-
 11 READ.RAM.+



SAD.00-23 02



3 □ R.A.D. 20-31.+
 2 □ S.A.D. 20-31.+
 14 □ RAV RAS.D.-
 14 □ RAV CAS.D.-
 14 □ RAV WEN.C.-

14 □ RAV RAS.C.-
 14 □ RAV CAS.C.-

14 □ RAV WEN.D.-

9 □ RAM ECC.X.+
(x=0-6)

11 □ READ RAM.-

11 □ READ RAM.+

2.A.D.D. 20.+ 5 A0
 31.+ 6 A1
 32.+ 7 A2
 33.+ 12 A3
 34.+ 11 A4
 35.+ 10 A5
 36.+ 13 A6
 R.ADD. 37.+ 9 A7
 2 CAS
 15 CAS
 3 WEN
 2 DIN DOUT

2.A.D.D. 30.+ 5 A0
 31.+ 6 A1
 32.+ 7 A2
 33.+ 12 A3
 34.+ 11 A4
 35.+ 10 A5
 36.+ 13 A6
 R.ADD. 37.+ 9 A7
 2 CAS
 15 CAS
 3 WEN
 2 DIN DOUT

2.A.D.D. 30.+ 5 A0
 31.+ 6 A1
 32.+ 7 A2
 33.+ 12 A3
 34.+ 11 A4
 35.+ 10 A5
 36.+ 13 A6
 R.ADD. 37.+ 9 A7
 2 CAS
 15 CAS
 3 WEN
 2 DIN DOUT

RAM.ECC.0.+ 2
 2 DIN DOUT

745241
 1 OE1
 18 OE2
 11
 6
 3
 6
 15
 2
 17
 2
 LC

745241
 19
 6
 11
 13
 6
 4
 17
 2
 PU2
 3A

2 S.A.D. 24.+ 9
 25.+ 12
 26.+ 7
 27.+ 12
 28.+ 5
 29.+ 16
 30.+ 3
 31.+ 18
 S.A.D. 24-31.+ 02

R.ECC.0-6.+ 04,9
 12 R.ECC.0.+
 9 1.+
 7 2.+
 14 3.+
 5 4.+
 16 5.+
 3 R.ECC.6.+
 18

R.OUT.20-23.+ 5

S.A.D. 00+
(xx=00-31)

C. DATA .xx-
(xx=0-31)

ECC. SYN 0+
1-
ECC. SYN 2+

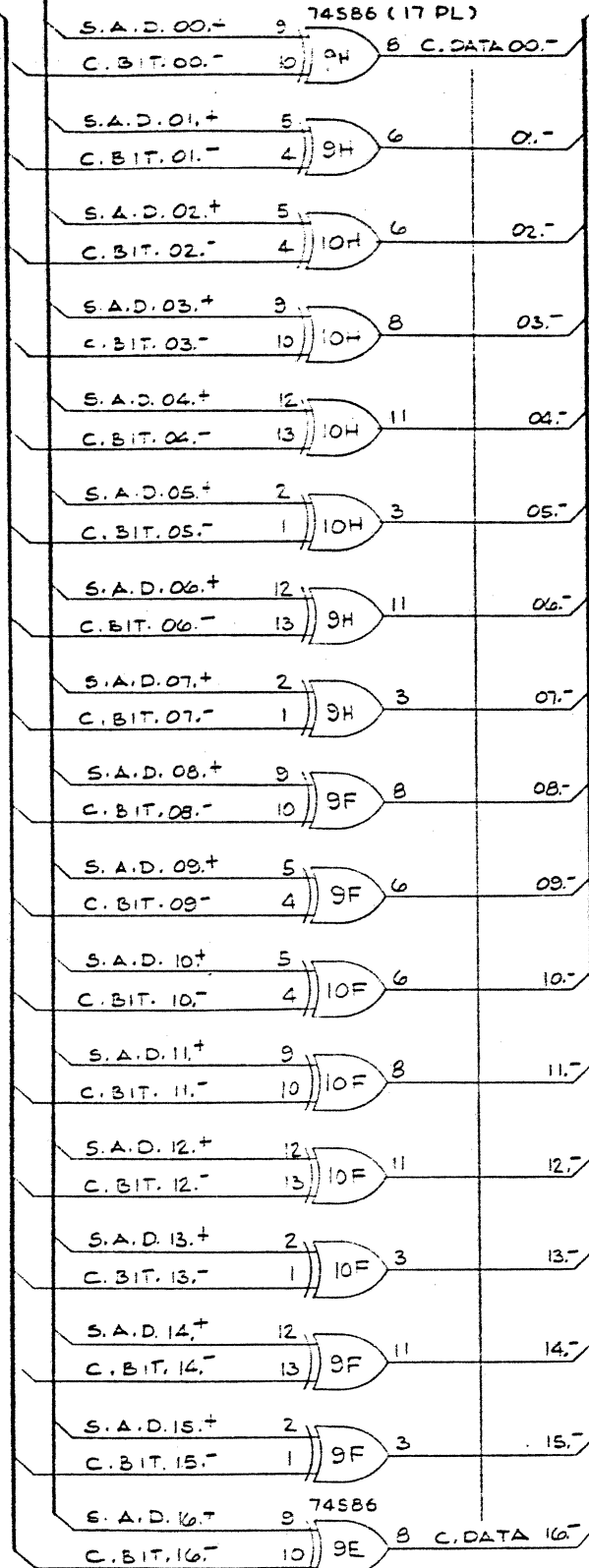
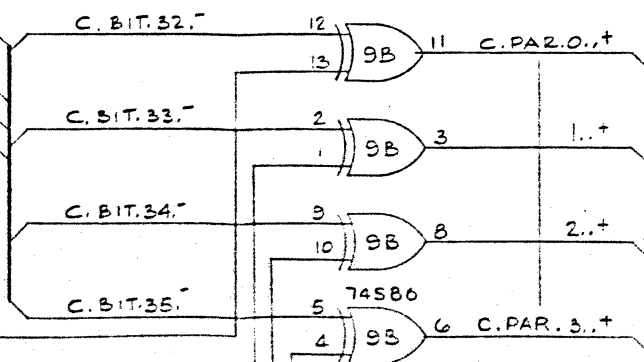
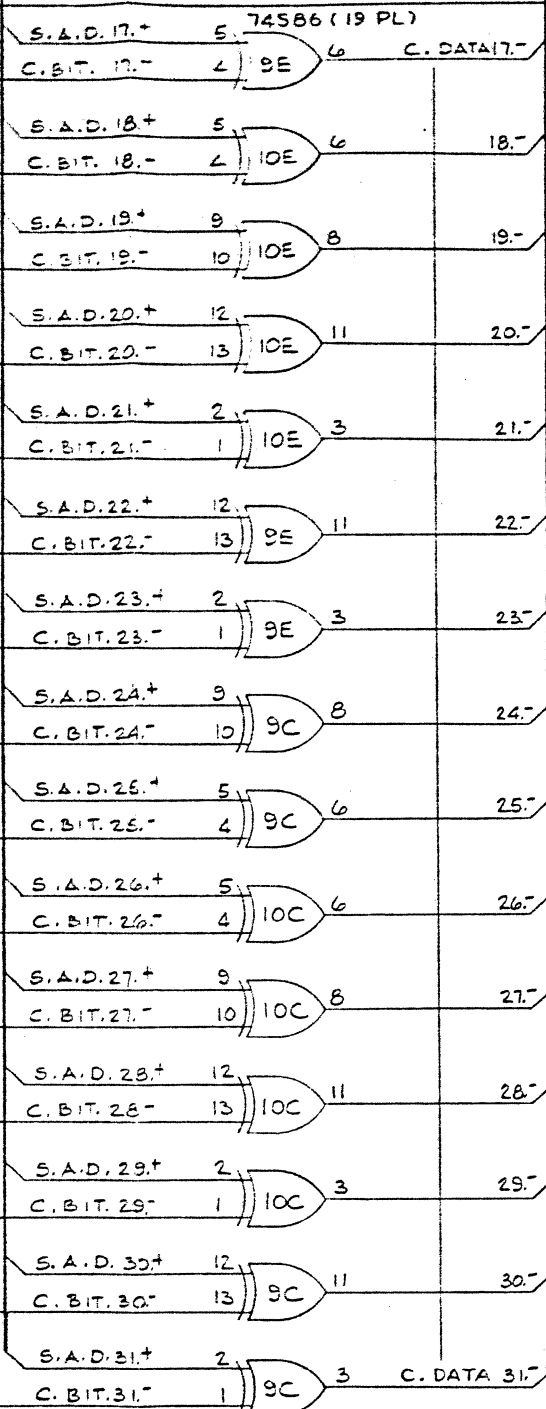
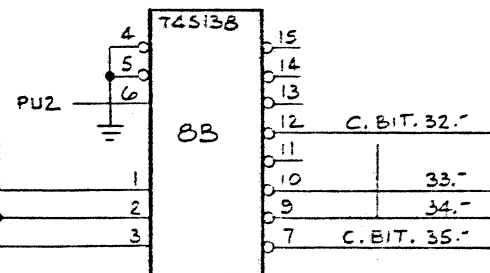
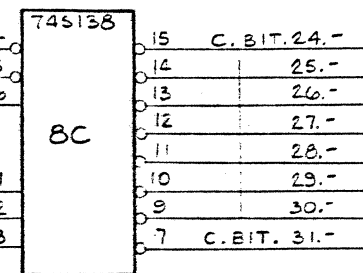
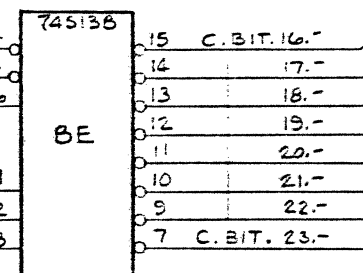
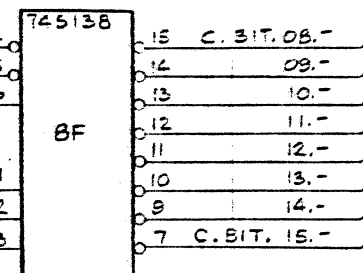
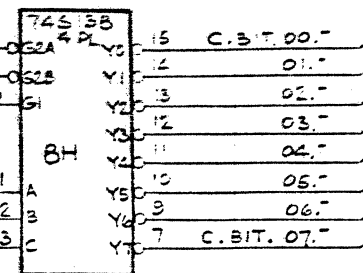
ECC. SYN 3+

ECC. SYN 4+

ECC. SYN 5+

ECC. SYN 3+
2-
ECC. SYN 5+

PAR. BIT 0+
1-
2-
PAR. BIT 3+

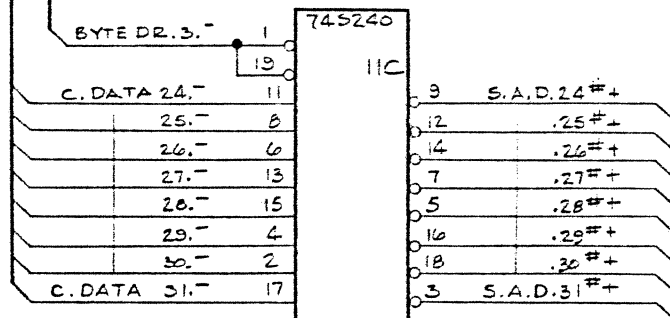
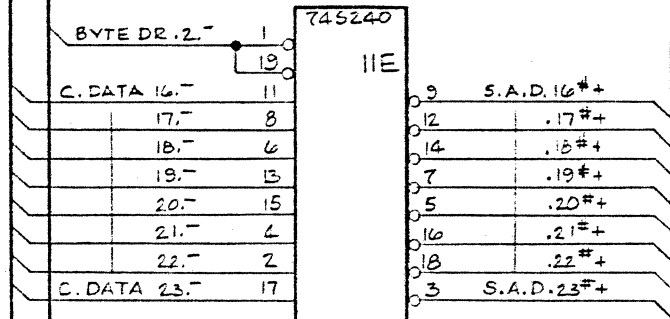
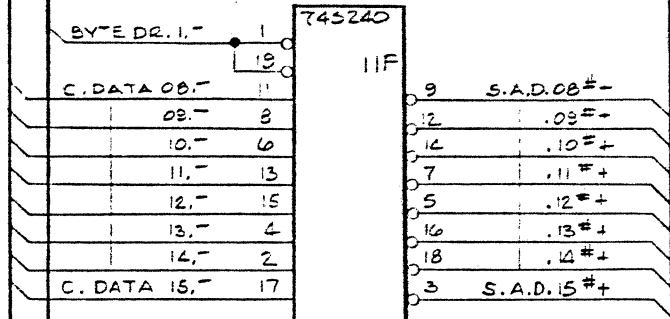
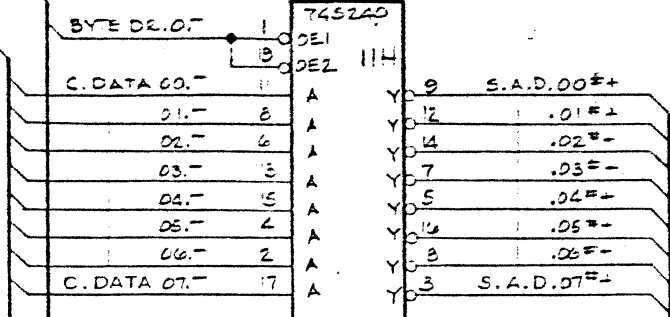
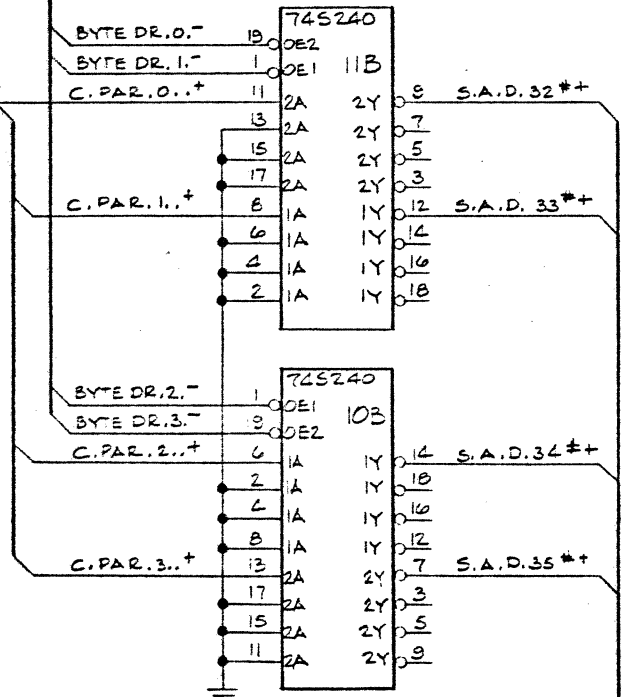


C. PAR. Y...+
(x=0-3)

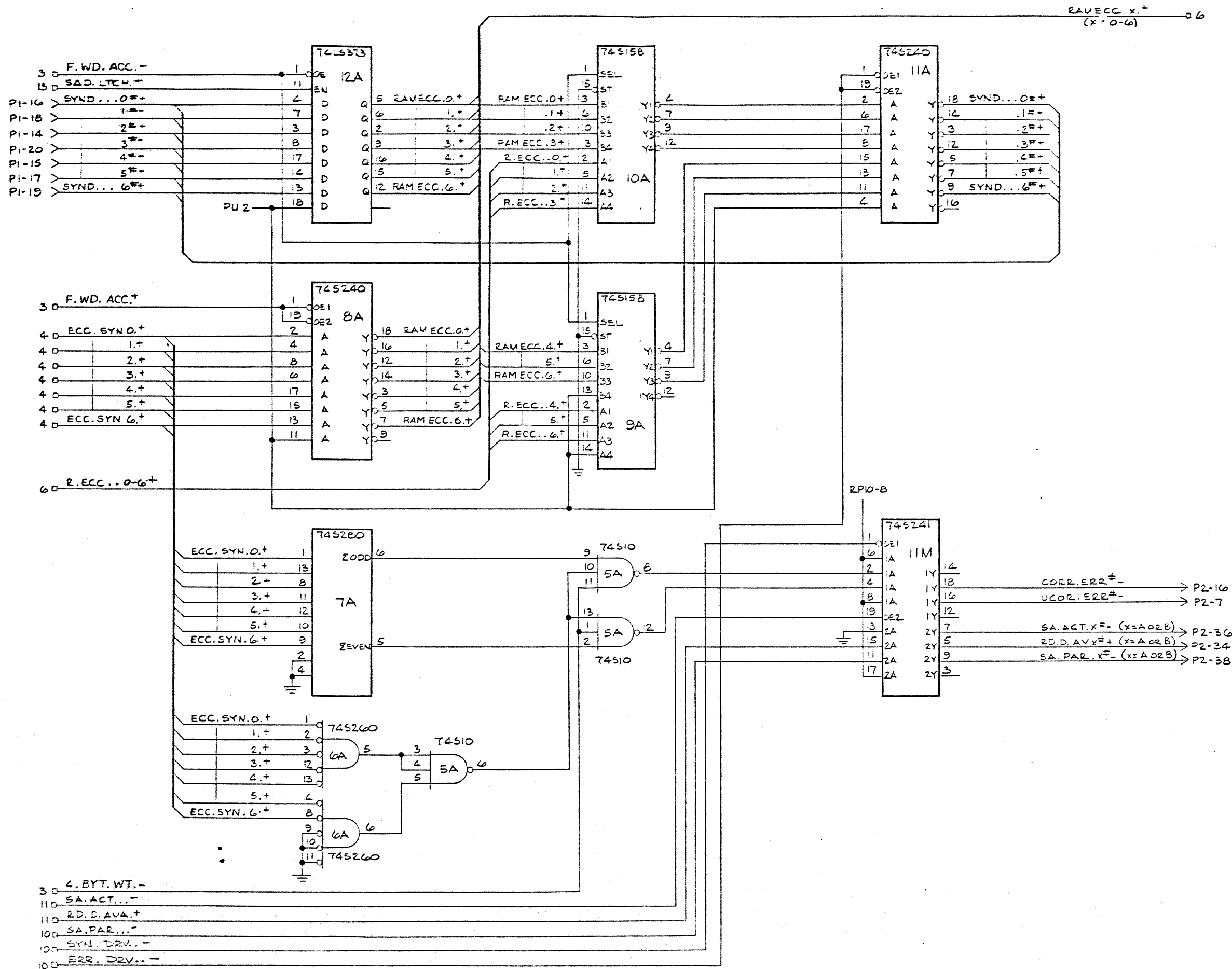
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D	112338	7	C

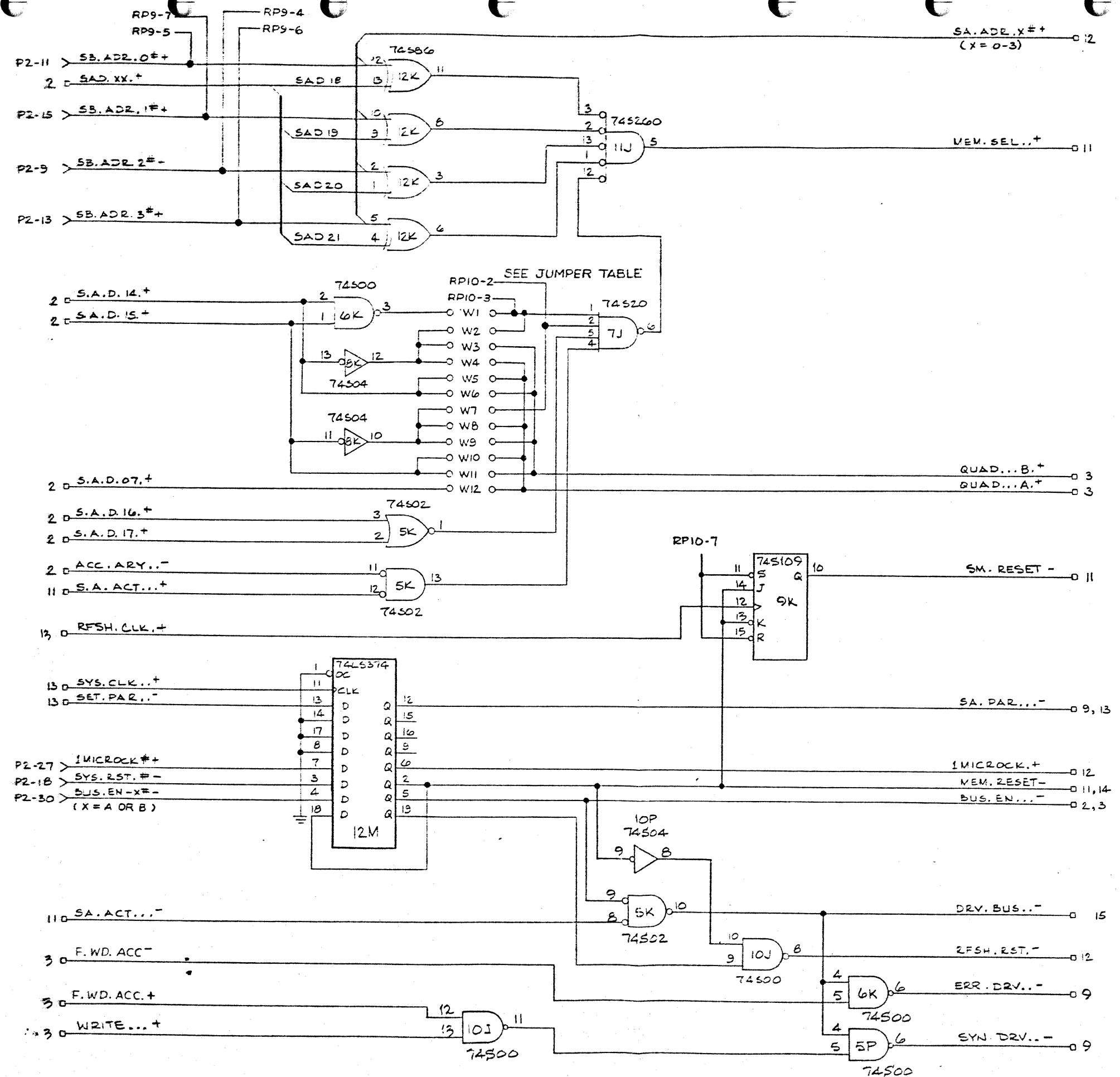
3 0 BYTE DR. Y.
(X=0-3)
7 0 C. DATA XX.
(XX=0-31)

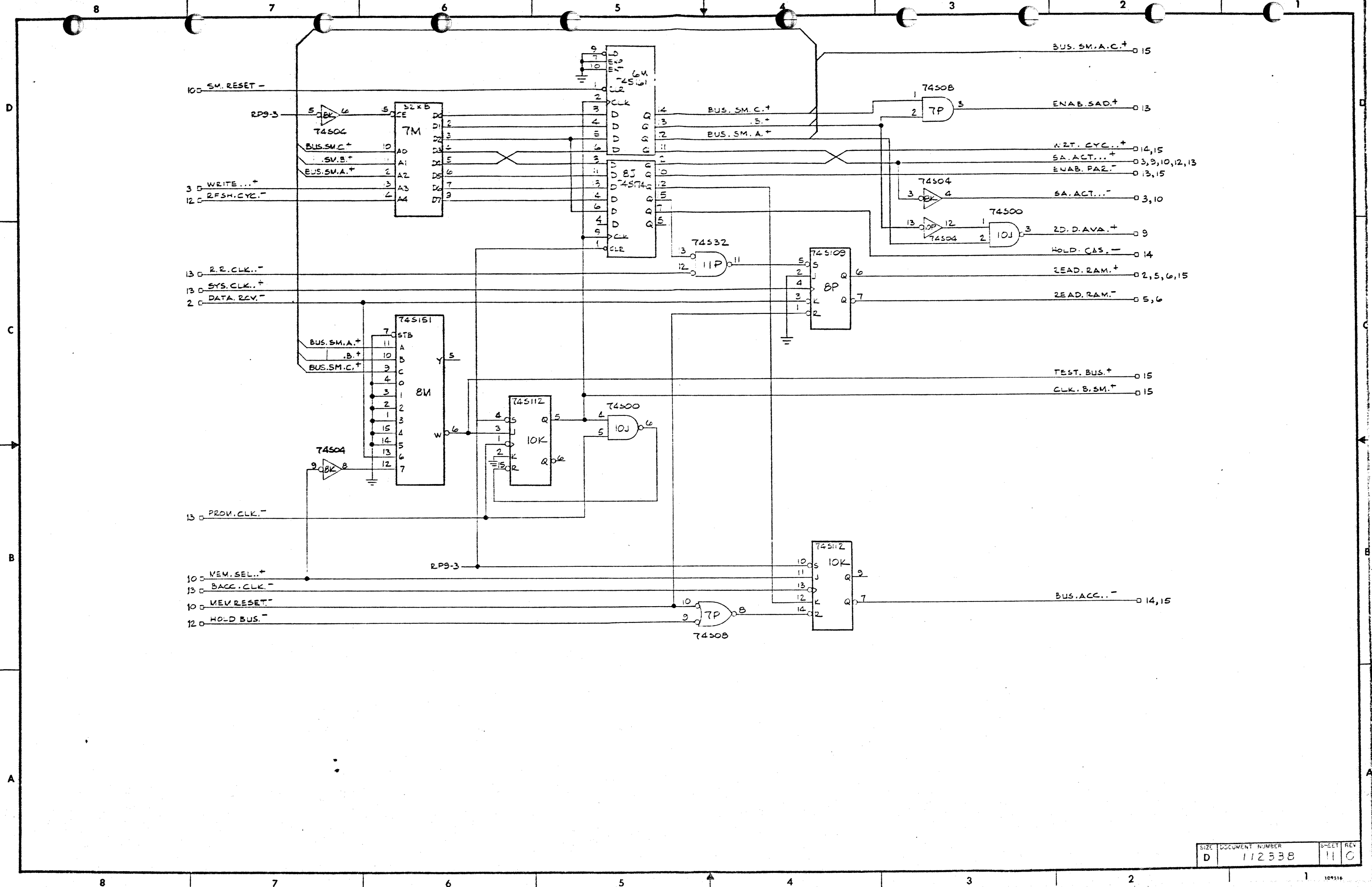
7 0 C. PAR. Y.
(X=0-3)



S.A.D. XX**
(XX = 00-31) □ 2
S.A.D. XX**
(XX = 32-35) □ 2





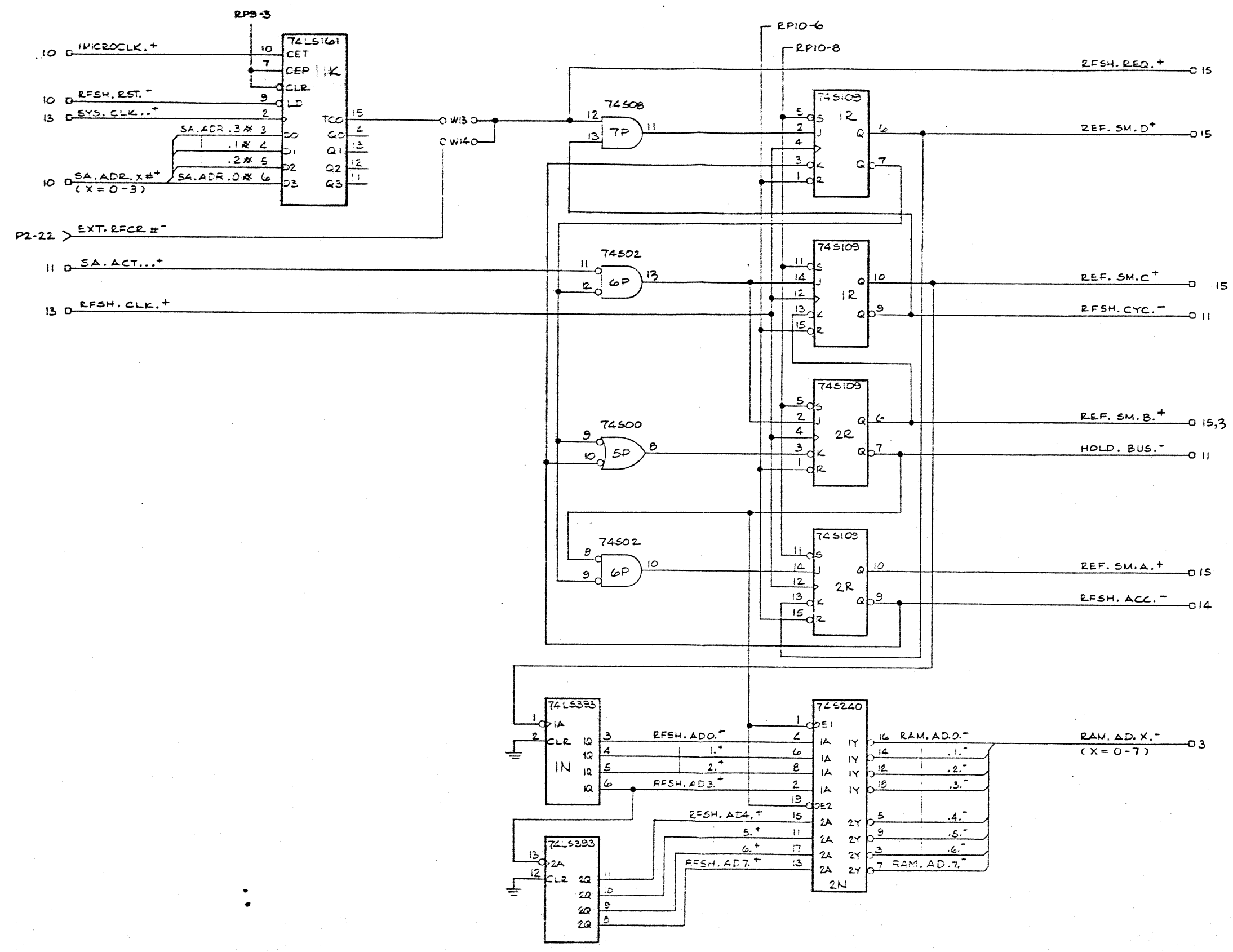


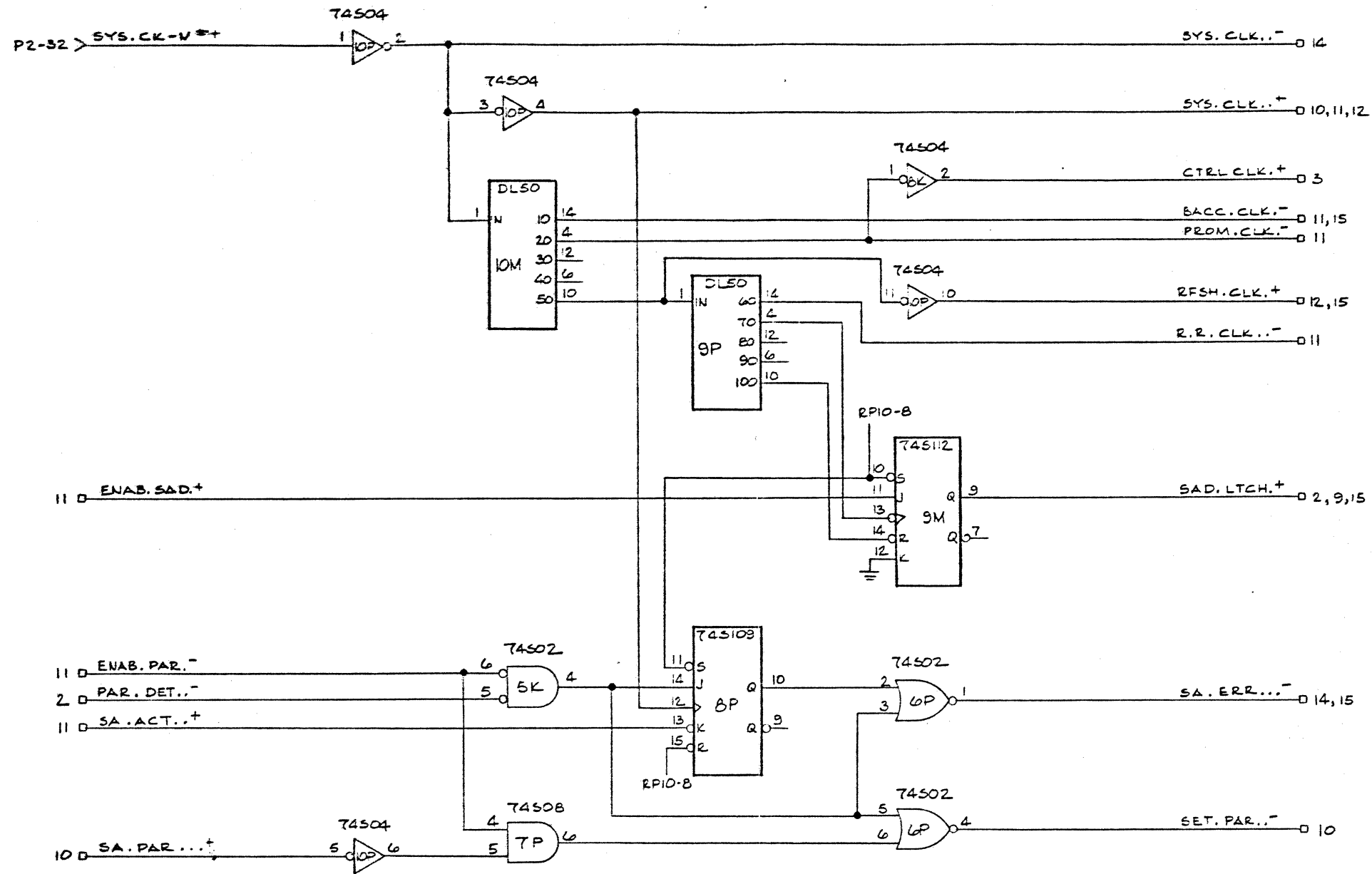
D

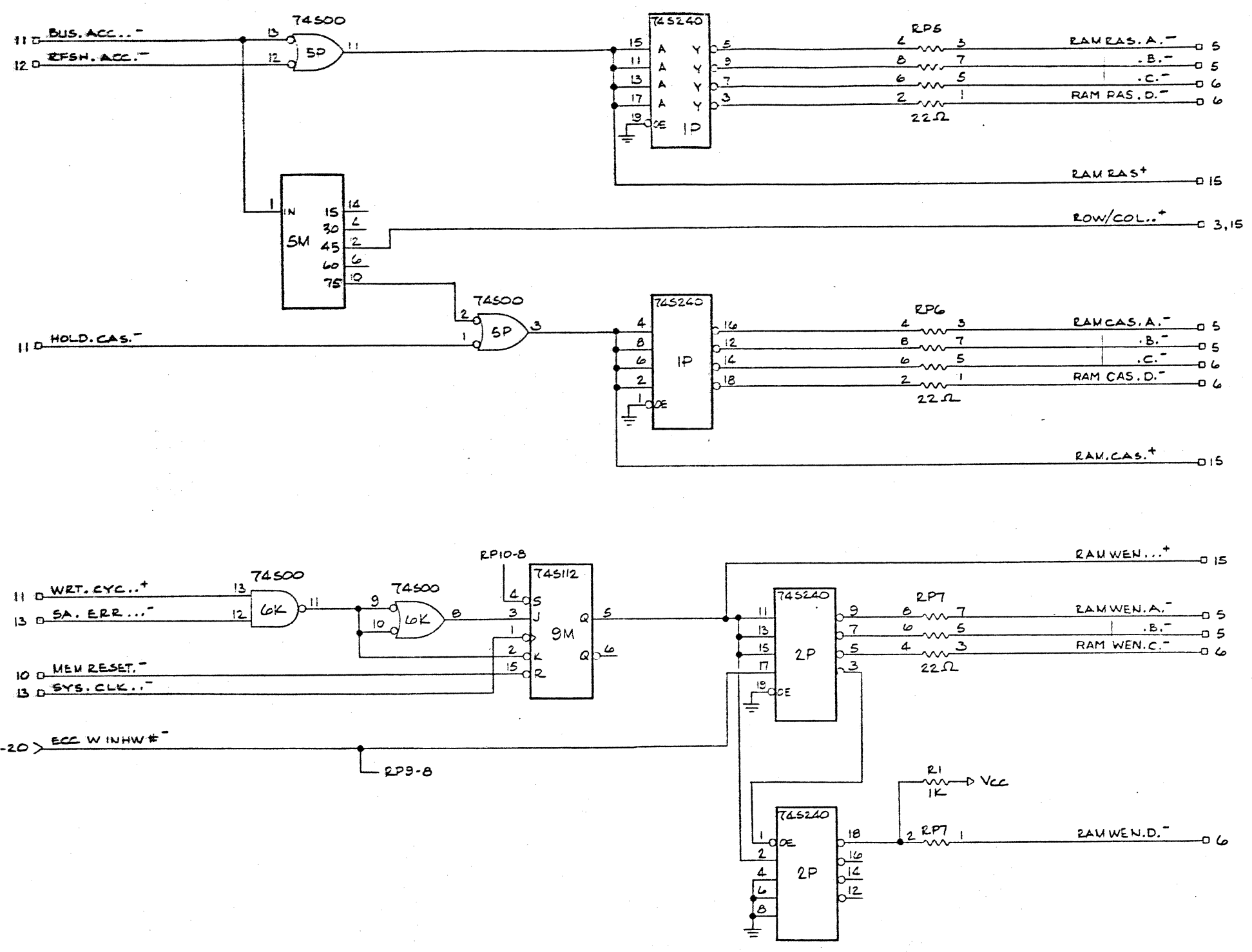
C

B

A







13	0	SAD LATCH. +	E1	} BUS CONTROL GROUP
11	0	READ. RAM. +	E2	
10	0	DRV. BUS. -	E3	
3	0	BYTE DR. 0. -	E4	
3	0	.1. -	E5	
3	0	.2. -	E6	
3	0	BYTE DR. 3. -	E7	

3	0	WRITE +	E8	} SYS BUS SM GROUP
11	0	BUS. SM. A.	E9	
11	0	.B.	E10	
11	0	BUS. SM. C.	E11	
11	0	CLK. B. SM. +	E12	
11	0	TEST. BUS -	E13	
11	0	WRT. CYC. +	E14	
11	0	BUS. ACC. -	E15	
13	0	BACC. CLK. -	E16	

12	0	RFSH. REQ. +	E17	} REFRESH SM GROUP
12	0	REF. SM. A. +	E18	
12	0	.B. +	E19	
12	0	.C. +	E20	
12	0	REF. SM. D. +	E21	
13	0	RFSH. CLK. +	E22	

14	0	RAMRAS... +	E23	} RAM CONTROL SM GROUP
14	0	ROW/COL... +	E24	
14	0	RAMCAS... +	E25	
14	0	RAMWEN... +	E26	

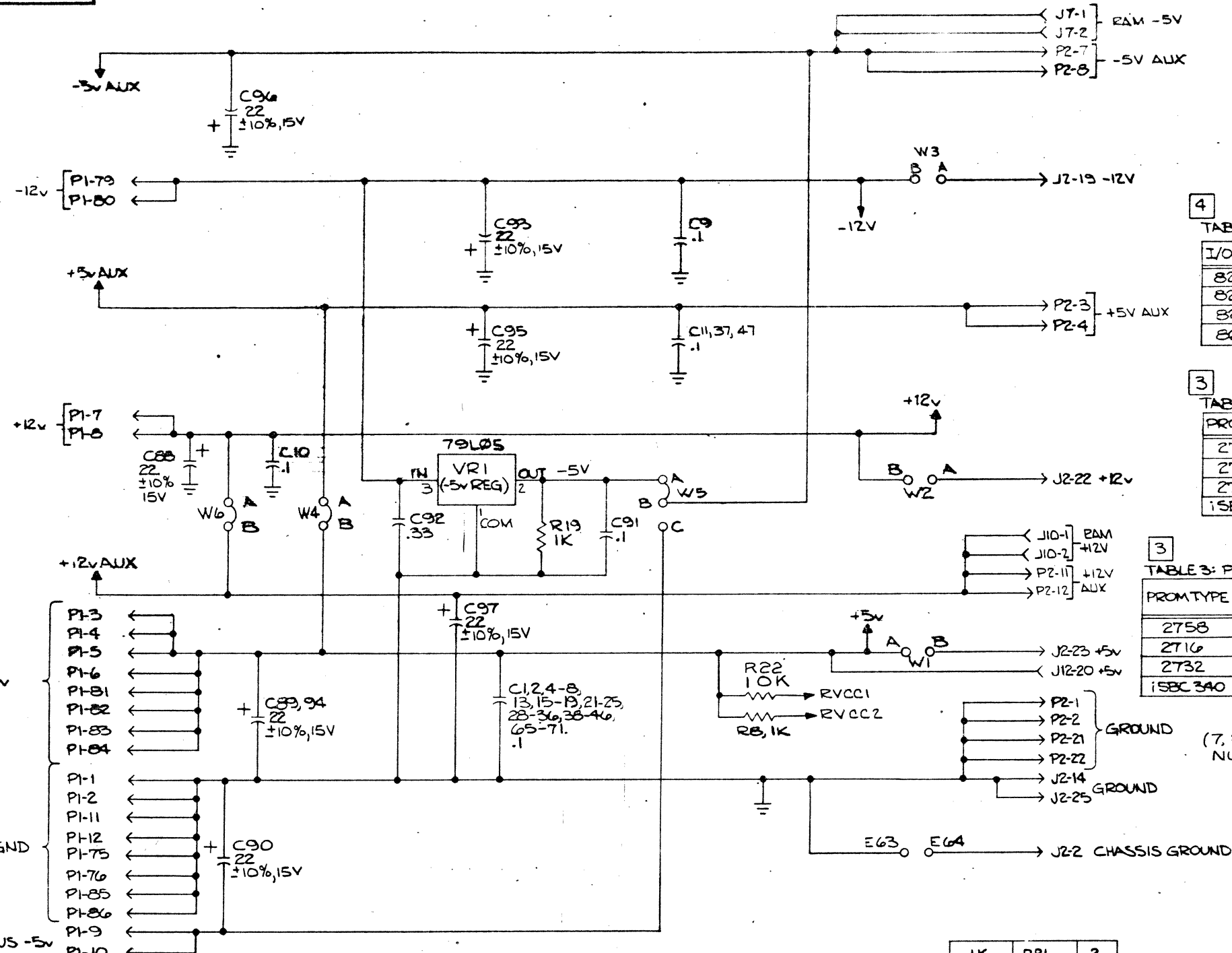
2	0	PAR. DET. -	E27	} BUS PARITY GROUP
11	0	ENAB. PAR. -	E28	
13	0	SA. ERR... -	E29	

4	0	ECC. SYN 0. +	E30	} ECC & SYNDROME CODE
4	0	.1. +	E31	
4	0	.2. +	E32	
4	0	.3. +	E33	
4	0	.4. +	E34	
4	0	.5. +	E35	
4	0	ECC. SYN 6. +	E36	

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DWG NO. 143377

ZONE	REV	DESCRIPTION	DFT	CHK	DATE	APPROVED
E		ECO 40-2954			11/16/81	HL



POWER AND GROUND LOCATOR CHART

REF DES	DEVICE TYPE	POWER PINS				
		GROUND	+5v	-5v	+12v	-12v
VR1	79L05	1	-	2	-	3
A30,57	74LS75	12	5	-	-	-
A16	74163	8	16	-	-	-
A56	7425	7	14	-	-	-
A4,49	74S175	8	16	-	-	-
A86	74S240	10	20	-	-	-
A40,41,71,91	74S373	10	20	-	-	-
A55	74S30	7	14	-	-	-
A2,21,53	74S32	7	14	-	-	-
A14	75189	7	14	-	-	-
A15	75188	7	-	-	14	1
A19,32	74S08	7	14	-	-	-
A18,54	74S139	8	16	-	-	-
A64	74S140	7	14	-	-	-
A35,84,85	74LS04	7	14	-	-	-
A3,7	74S10	7	14	-	-	-
A65	8097	8	16	-	-	-
A1,37,62	74125	7	14	-	-	-
A48	7438	7	14	-	-	-
A20,34	74S04	7	14	-	-	-
A23	74S02	7	14	-	-	-
A50,63	74S74	7	14	-	-	-
A6,31	74S11	7	14	-	-	-
A31,33,52	74S00	7	14	-	-	-
A22	7432	7	14	-	-	-
A66	74LS138	8	16	-	-	-
A5	9602	8	16	-	-	-
A36	74LS00	7	14	-	-	-
A82	8289	10	20	-	-	-
A81,83	8288	10	20	-	-	-
A69,87,90	8287	10	20	-	-	-
A42,44,45,58,60,61	8286	10	20	-	-	-
A38	8284A	9	18	-	-	-
A39	8086	1,20	40	-	-	-
A67,68	3625-2	9	18	-	-	-
A27	8251A	4	26	-	-	-
A25	8255A	7	26	-	-	-
A26	8253	12	24	-	-	-
A24	8259A	14	28	-	-	-
A30	8224	8	16	-	-	-
A8,9	8226	8	16	-	-	-

TABLE 1: I/O ADDR SELECT

I/O DEVICE	BASE ADDR
8255A	00CB
8259A	00C0
8253	00D0
8251A	00DB

TABLE 2: PROM SELECT

PROM TYPE	ADR FROM
2758	FF00
2716	FE00
2732	FC00
15BC 340	FB00

TABLE 3: PROM SELECT

PROM TYPE	94 TO	97 TO	S1 0-9	S1 7-10
2758	95	98	C	C
2716	96	98	C	0
2732	96	99	0	C
15BC 340	96	99	0	0

O = OPEN
C = CLOSED
(7, 8, 9 AND 10 ARE PIN NUMBERS OF S1)

REF. DESIGNATIONS	VALUES	TYPE	REF. DES.	QTY	
P2	1K	RPI	2		
C98	1K	RP2	4		
E152	10K	RP3	2		
CR2	C14, 85		74S175	A49	1
A99	E2, 109, E100, 101, 102, 110, 111, 146-150		7438	A48	1
J13	A10, 11, 12, 13, A28, 29, 46, 47		74LS75	A30	1
R23	J4, 8, 11		74125	A62	1
R24	R6		7432	A59	2
Y3	R10		74S32	A21	1
S1	R12		9602	A5	1
VR1			74S175	AA	1
W9					

- NOTES: UNLESS OTHERWISE SPECIFIED
- ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 WATT.
 - ALL CAPACITANCE VALUES ARE IN MICROFARADS, +30%, -20%, 50VDC.
 - SEE TABLES 2 AND 3 FOR PROM SELECTION.
 - SEE TABLE 1 FOR I/O SELECTION.

UNLESS OTHERWISE SPECIFIED:

- DIMENSIONS ARE IN INCHES.
- BREAK ALL SHARP EDGES.
- DO NOT SCALE DRAWING.
- TOLERANCES: ANGLES ± 2°, XX ± .030, XXX ± .010

QUANTITY PER DASH NO.

ITEM NO. PART NUMBER DESCRIPTION

SIGNATURE DATE

DRN BY: [Signature] DATE: [Date]

CHK BY: [Signature] DATE: [Date]

ENGR. APVD: [Signature] DATE: [Date]

APVD

APVD

INTEL

3065 BOWERS AVE. SANTA CLARA CALIF. 95051

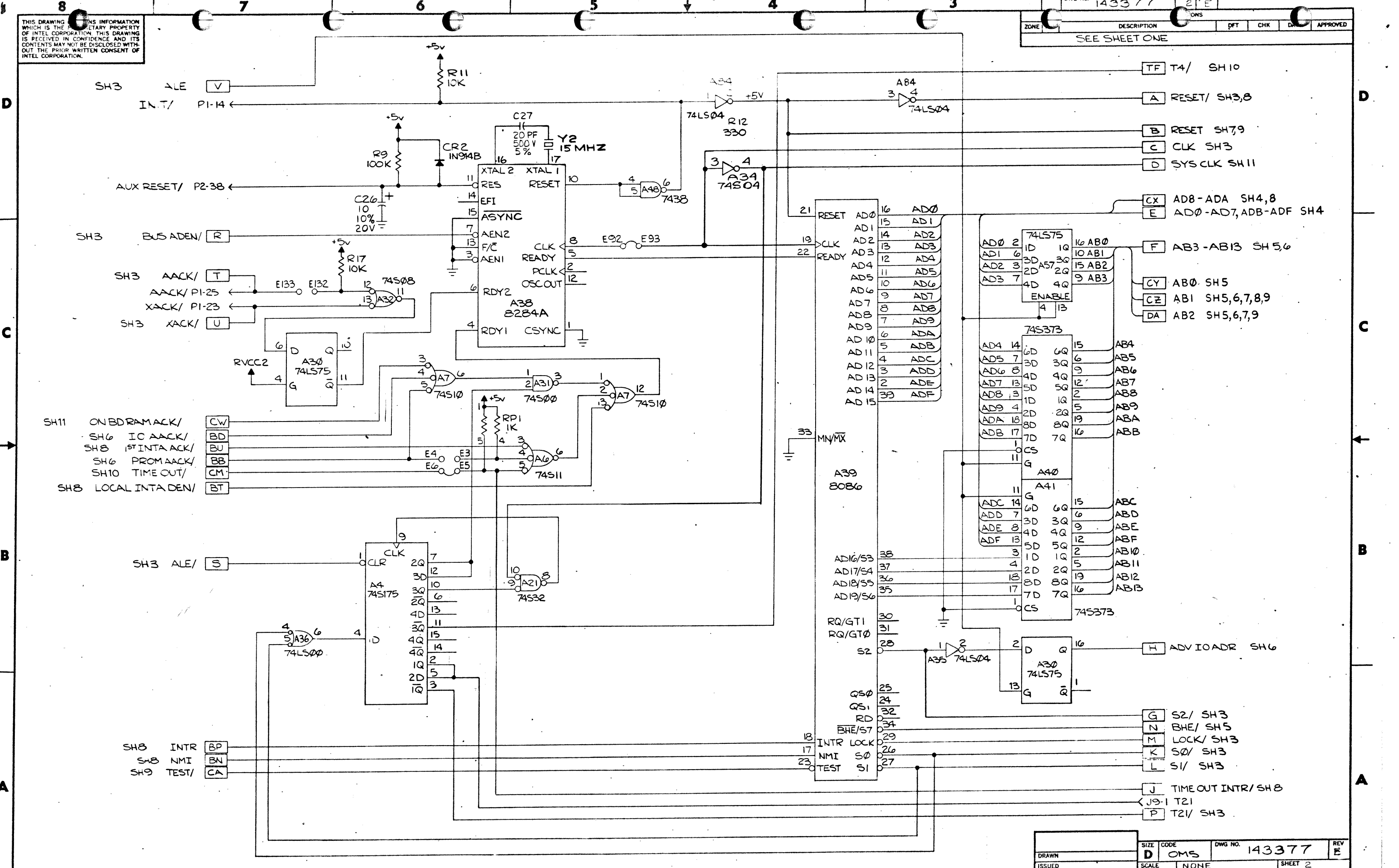
TITLE: SCHEMATIC DIAGRAM, 15BC 86/12A

SIZE CODE DWG. NO. REV

D OMS 143377 E

SCALE NONE SHEET 1 OF 11

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D

D

C

C

B

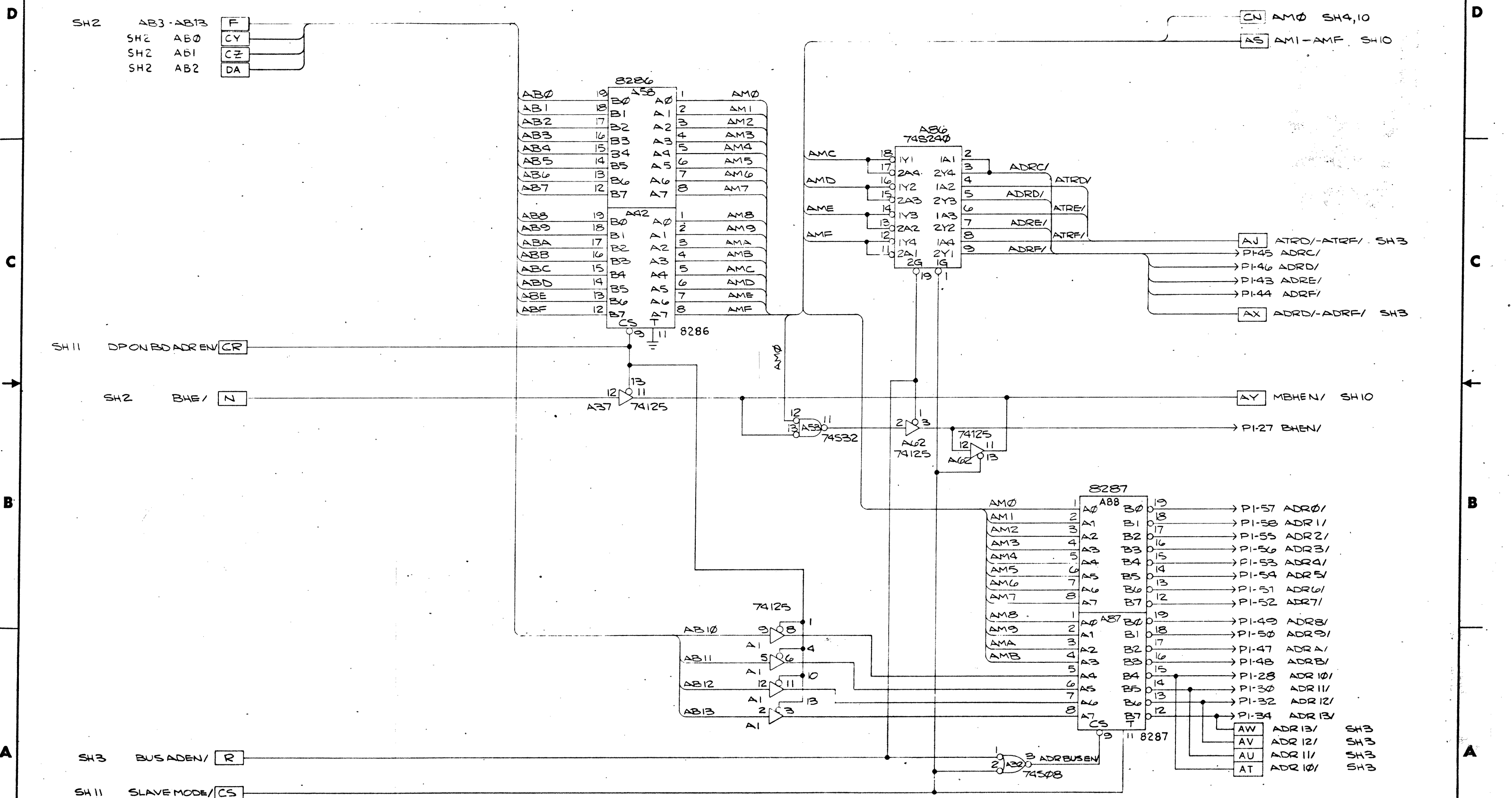
B

A

A

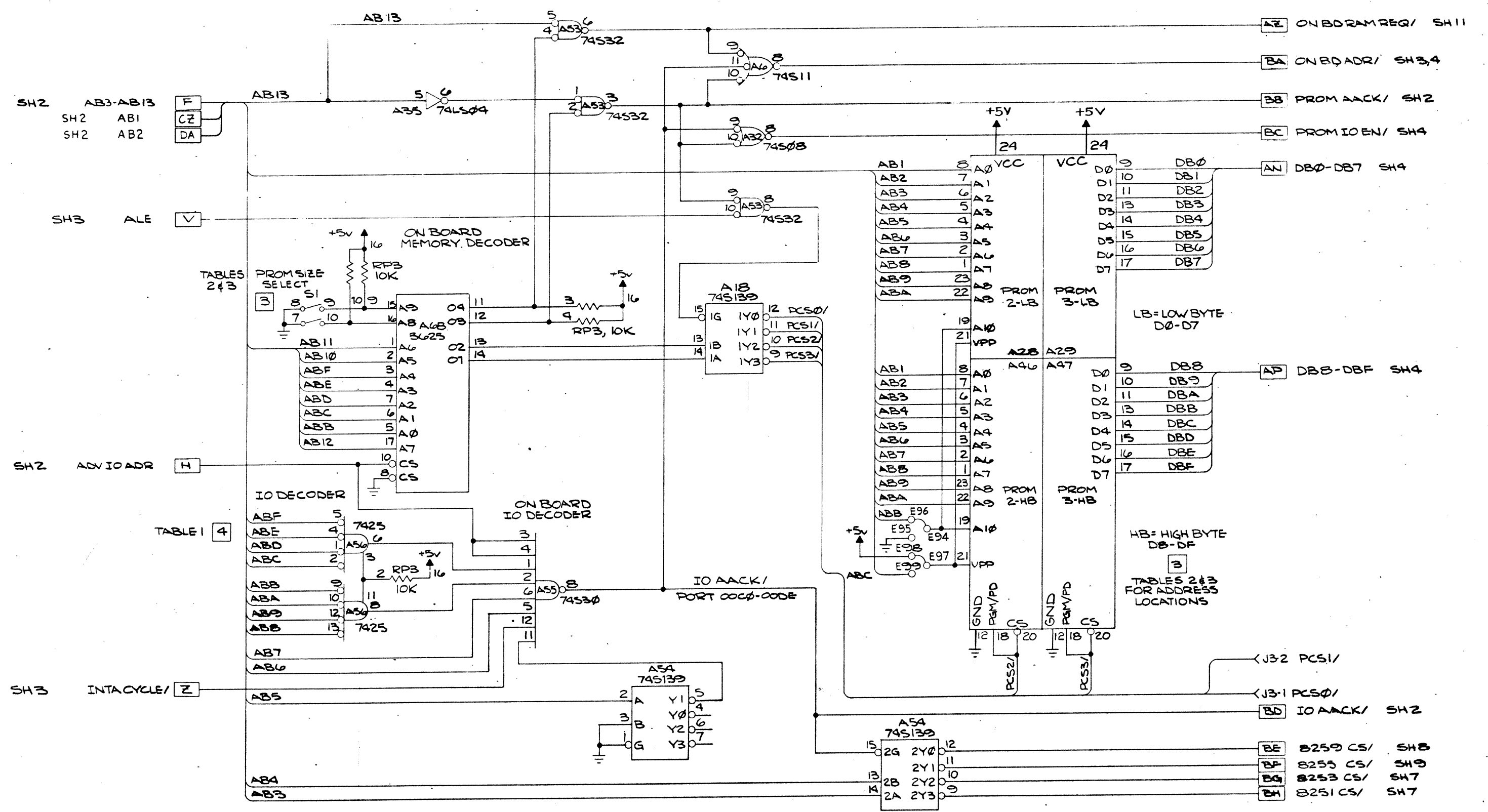
THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

DWG NO 143377		REV E	
ZONE	REV	DESCRIPTION	DATE
		SEE SHEET ONE	



SIZE	CODE	DWG NO	REV
D	0MS	143377	E
ISSUED	SCALE	NONE	SHEET

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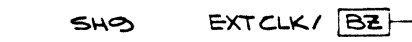
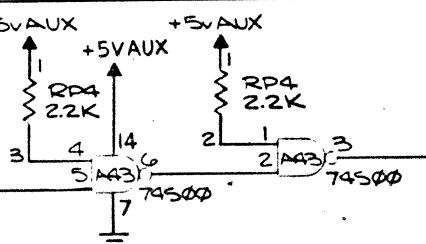
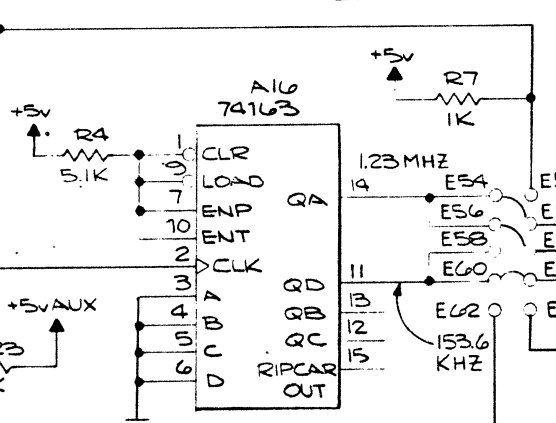
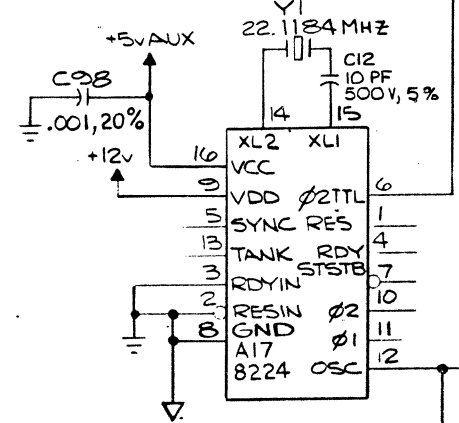
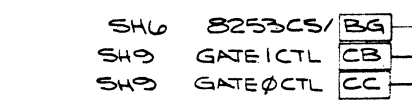
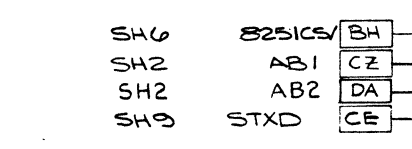
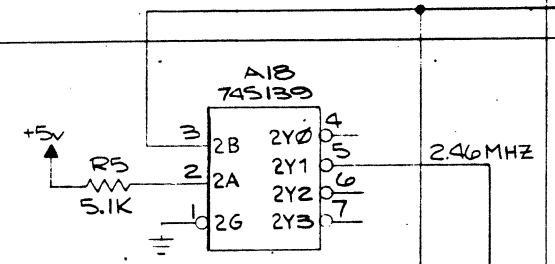
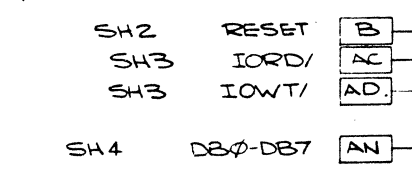
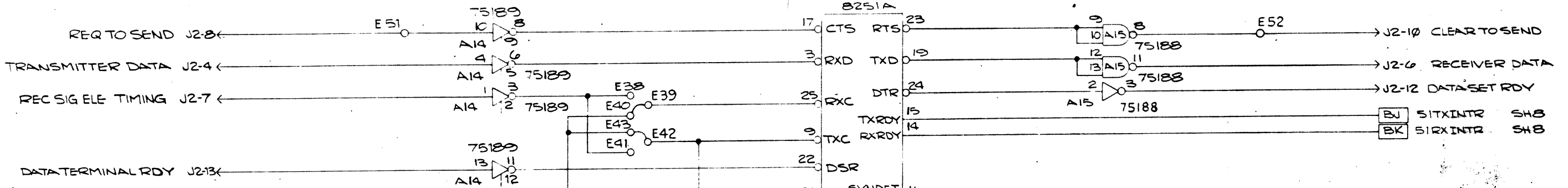
PORT NO.	FUNCTION
00DB	DATA
00DA	CONTROL

A27
8251A

PORT NO.	FUNCTION
00DB	DATA
00DA	CONTROL
00D0	COUNTER 0
00D2	COUNTER 1
00D4	COUNTER 2
00D6	CONTROL

PORT NO.	FUNCTION
00D0	COUNTER 0
00D2	COUNTER 1
00D4	COUNTER 2
00D6	CONTROL

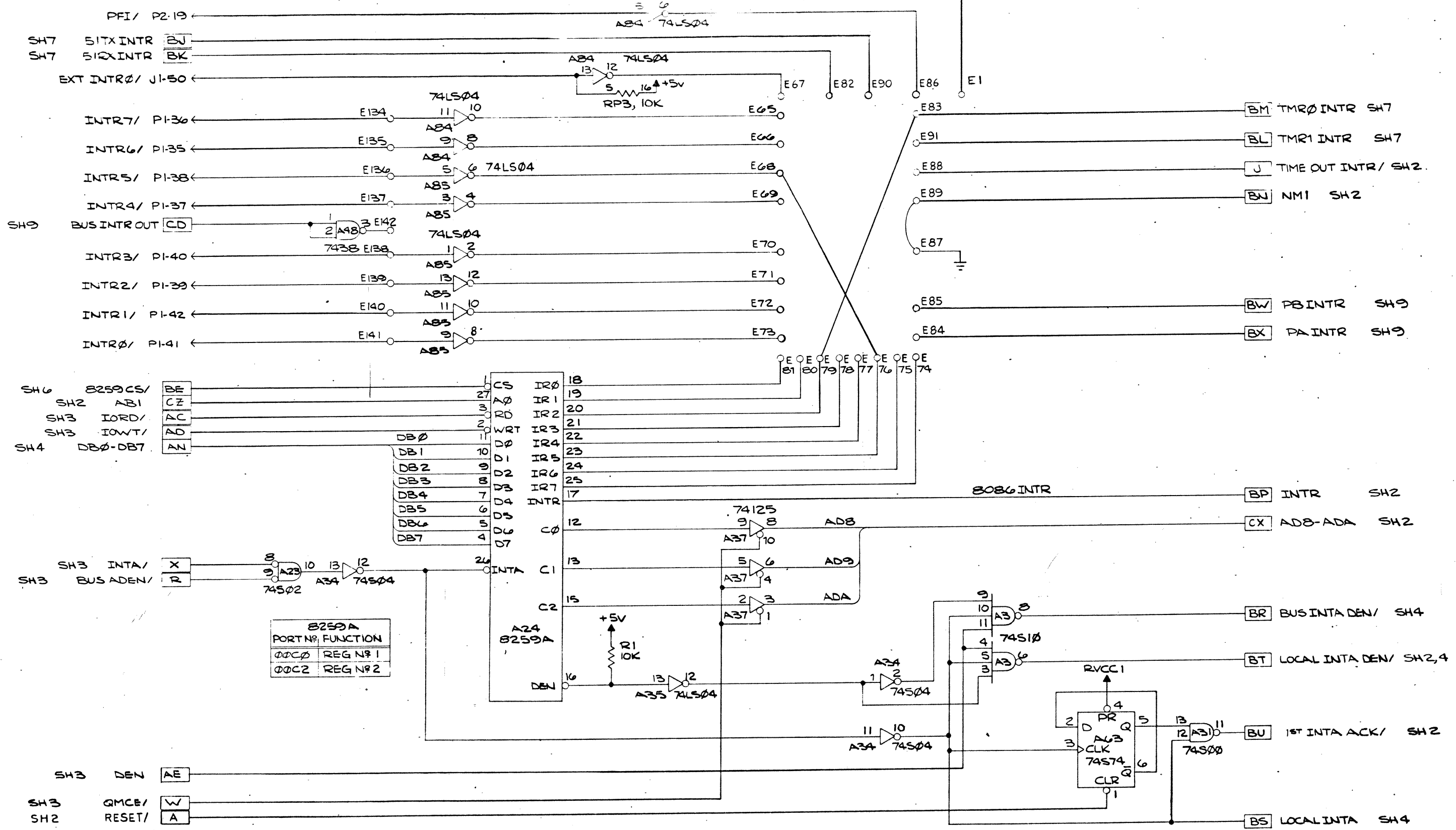
PORT NO.	FUNCTION
00D0	COUNTER 0
00D2	COUNTER 1
00D4	COUNTER 2
00D6	CONTROL



PORT NO.	FUNCTION
00D0	COUNTER 0
00D2	COUNTER 1
00D4	COUNTER 2
00D6	CONTROL

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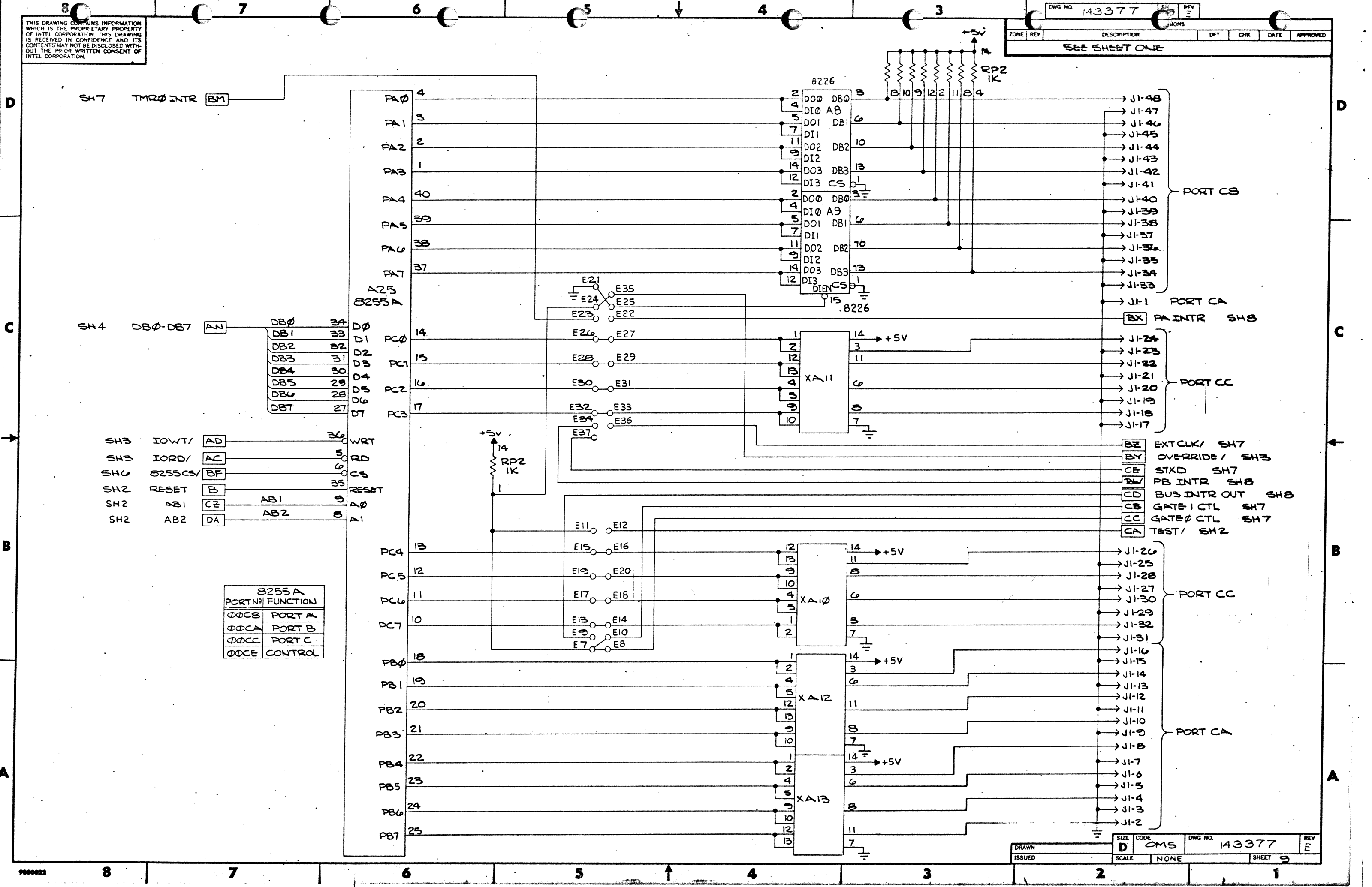
J13-1 MINT ←



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DWG NO. 143377

ZONE	REV	DESCRIPTION	DFT	CHK	DATE	APPROVED
SEE SHEET ONE						

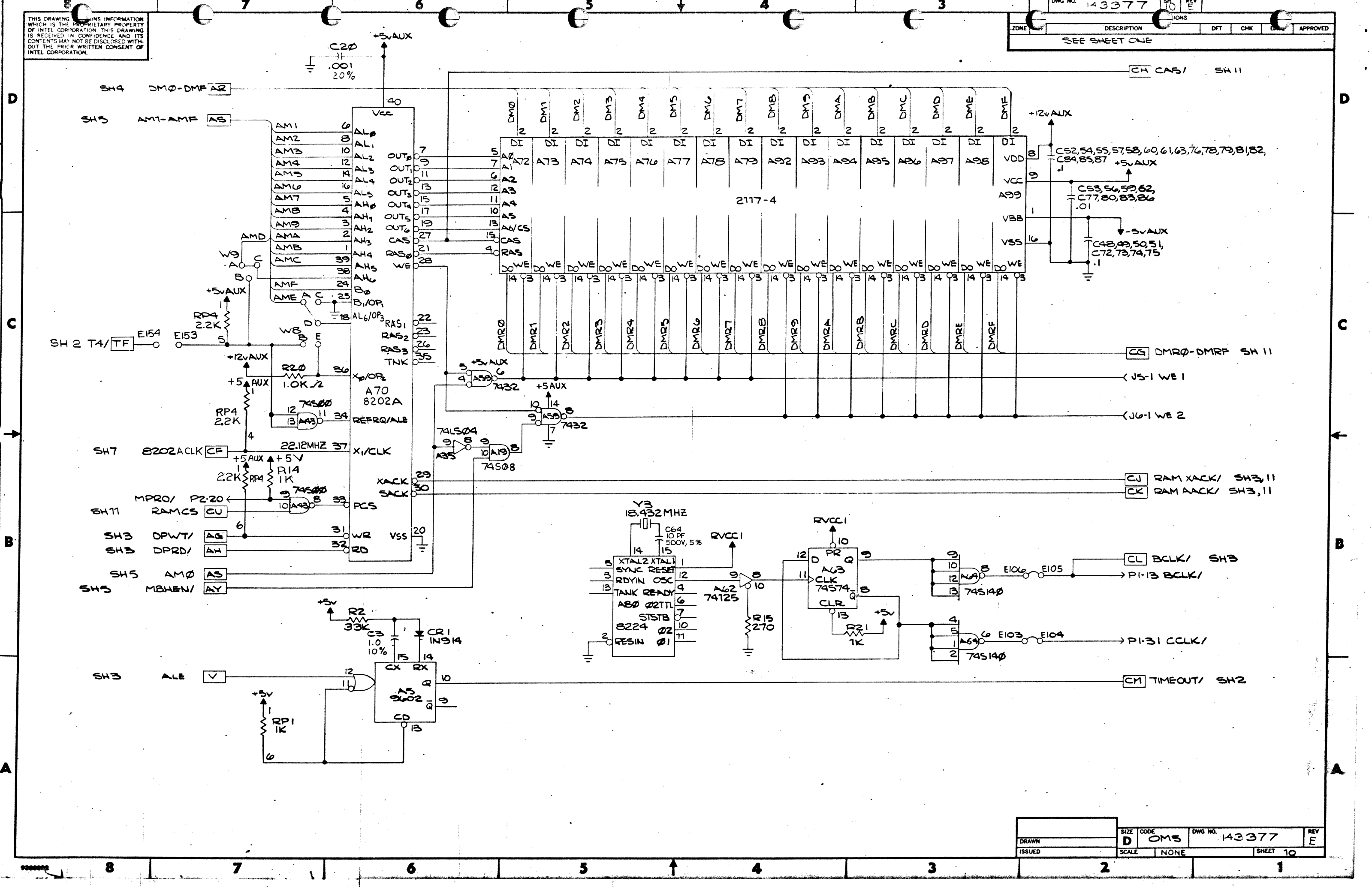


8255A	
PORT NO	FUNCTION
DB0-DB7	PORT A
DB8-DB15	PORT B
DB16-DB23	PORT C
DB24-DB27	CONTROL

DRAWN	ISSUED	SCALE	CODE	DWG NO.	REV
		NONE	OMS	143377	E

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DWG NO.	143377	REV	E
DESCRIPTION	SEE SHEET ONE		
ZONE		DFT	CHK
			APPROVED

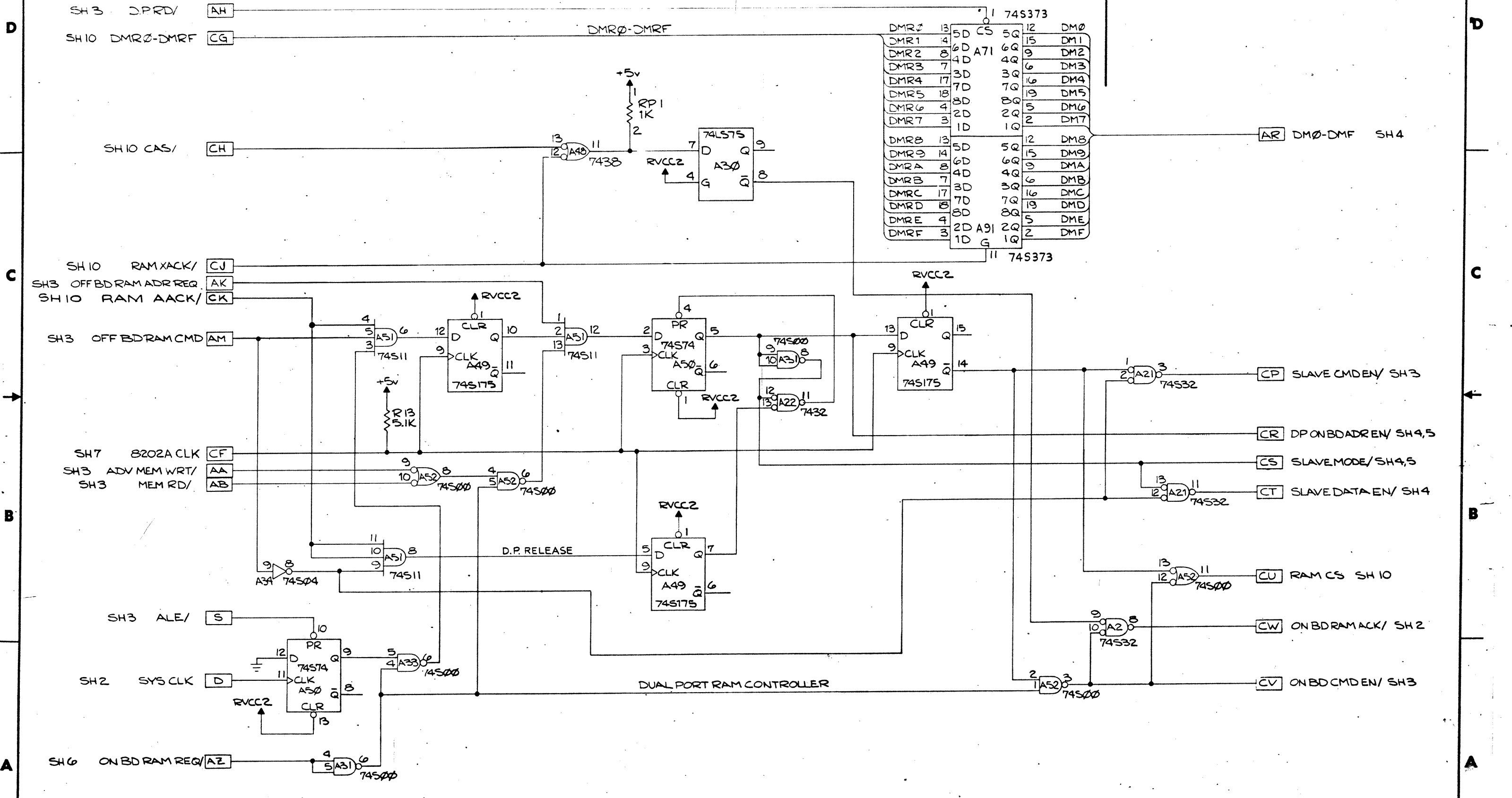


SIZE	CODE	DWG NO.	143377	REV	E
DRAWN	D	OM5			
ISSUED	SCALE	NONE	SHEET	10	

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DWG NO. 143377

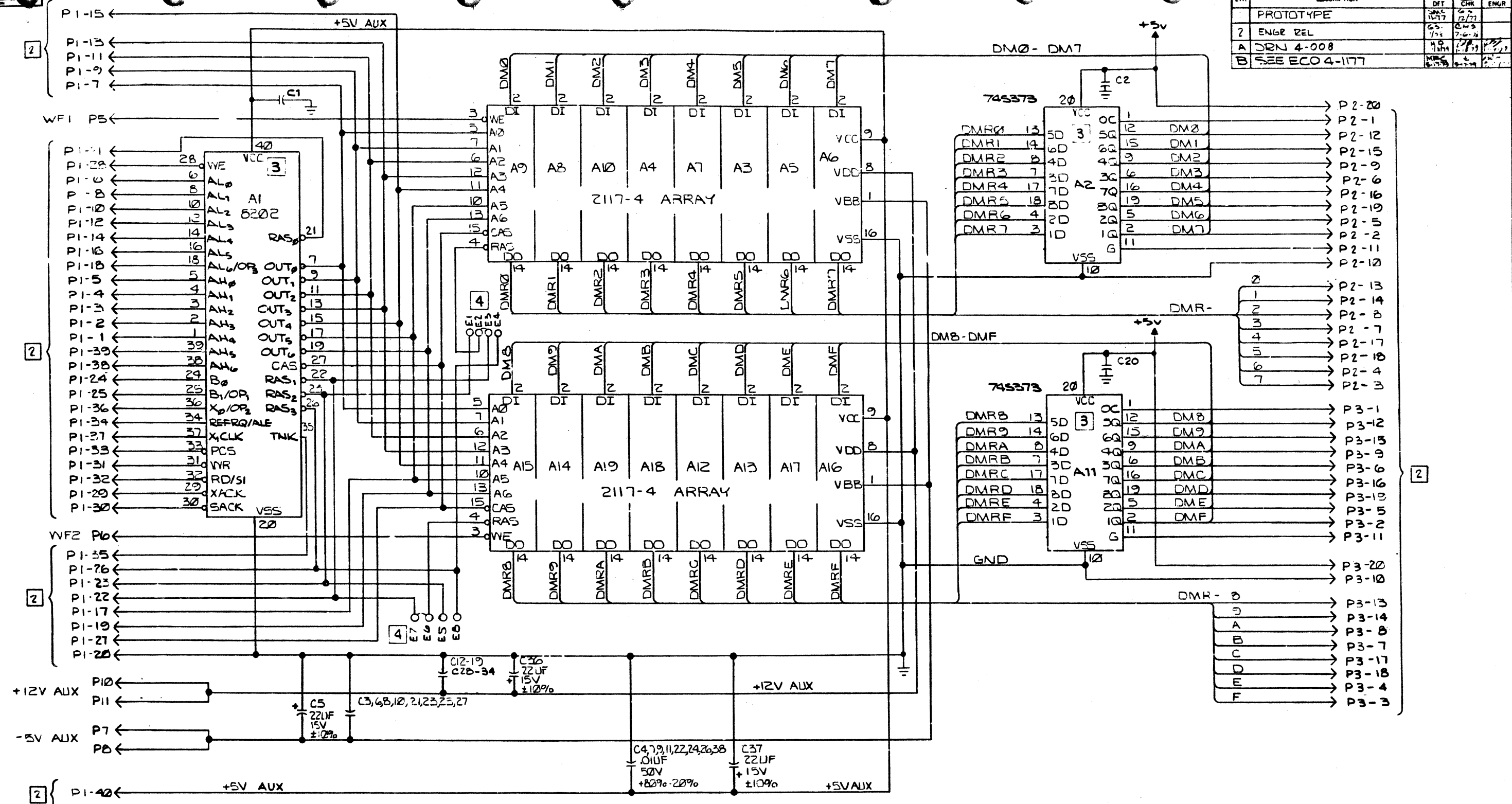
ZONE	REV	DESCRIPTION	DFT	CHK	DATE	APPROVED
SEE SHEET ONE						



DMR#	DMR1	DMR2	DMR3	DMR4	DMR5	DMR6	DMR7	DMR8	DMR9	DMRA	DMRB	DMRC	DMRD	DMRE	DMRF
13	4	8	7	17	18	4	3	13	14	8	7	17	8	4	3
5D	6D	4D	3D	7D	8D	2D	1D	5D	6D	4D	3D	7D	8D	2D	1D
CS	A71							5Q	6Q	4Q	3Q	7Q	8Q	2Q	1Q
12	15	9	6	16	19	5	2	12	15	9	6	16	19	5	2
DM0	DM1	DM2	DM3	DM4	DM5	DM6	DM7	DM8	DM9	DMA	DMB	DMC	DMD	DME	DMF

SIZE	CODE	DWG NO.	REV
D	OMS	143377	E
ISSUED	SCALE	NONE	SHEET 11

REVISIONS			
LTR	DESCRIPTION	SIGNATURE	DATE
	PROTOTYPE	WAS 1/77	1/77
2	ENGR REL	WAS 1/77	1/77
A	DRN 4-008	WAS 1/77	1/77
B	SEE ECO 4-1177	WAS 1/77	1/77



- NOTES: UNLESS OTHERWISE SPECIFIED
- CAPACITANCE VALUES ARE .1 MICROFARADS, +80%,-20%, 50V.
 - THESE (P) CONNECTIONS MATE WITH SOCKET ON MASTER BOARD.
 - IC'S A1, 2, 4, A11 ARE INSTALLED FROM MASTER BOARD.
 - JUMPER-HARDWARE CONNECTION.

RAS/ JUMPER TABLE			
RAS/ OF RAM FROM I8202	A3 TO A10 JUMPER E2 TO	A12 TO A19 JUMPER E4 TO	ES
RAS 1/	E3	E7	P11
RAS 2/	E1	E5	C38
RAS 3/	E4	ES	A19
			LAST USED NOT USED
			REF DESIGNATION

QUANTITY PER DASH NO.		ITEM NO.	PART NUMBER	DESCRIPTION
SCALE: NONE				
TOL: 2 PLC 3 PLC ANGLE				
MATERIAL:				
FINISH:				
SIGNATURE		DATE	PARTS LIST	
DRN BY: <i>WAS</i>		1/77	intel	
CHK BY: <i>WAS</i>		1/77	3065 BOWERS AVE. SANTA CLARA CALIF. 95051	
MATERIAL:			TITLE	
FINISH:			SCHEMATIC	
LAST USED NOT USED		1001798	LSBC 300 32K RAM MULTI MODULE	
REF DESIGNATION		300	SIZE DEPT DRAWING NO. REV	
			D OMS 2001800 B	

